Project code :91.3KF01.001
PCB No :12072
Revision :SB
Project Name :PIM70L-aPisa 20"/23"
Size : 150x240mm

aPisa_-1A Schematics Document

Ivy Bridge BGA1023 Intel Panther Point

aPisa_SB F7 Paramater

```
~ aPisa 20" CEL  UMA SKU : U,N
% aPisa 20" PDC  GPU SKU : G,U,N,O
~ aPisa 20" PDC  UMA SKU : U,N
~~~~~~~~~~~~~~~~~~~~~~~~~~
$ aPisa 23" I3   GPU SKU : S,G,A,H,O
```

aPisa_-1A F7 Paramater

```
%  aPisa 20" PDC  GPU SKU : G,U,N, (MarsXT)
~  aPisa 20" PDC  UMA SKU : U,N,O
~  aPisa 20" CEL  UMA SKU : U,N,O
%  aPisa 20" PDC  GPU SKU : G,U,N, (SunXT)
~~~~~~~~~~~~~~~~~~~~~~~~~~
$  aPisa 23" I3   GPU SKU : S,G,A,H,
&  aPisa 23" I3   UMA SKU : S,A,H,
```

R: Unmount
S: Scalar
G: GPU
U: UMA(NOT S)
A: AMP
N: non AMP
H: HDMI IN
O: OCP

GPU SKU:
Hynix R7419=8.45K(64.84515.6DL)
Samsung R7419=4.53K(64.45315.6DL)

OCP BOM manual control:
R1360,R1361,R1362,R1363 [63.R0031.16L]
Mount by BOM change list when w/o OCP

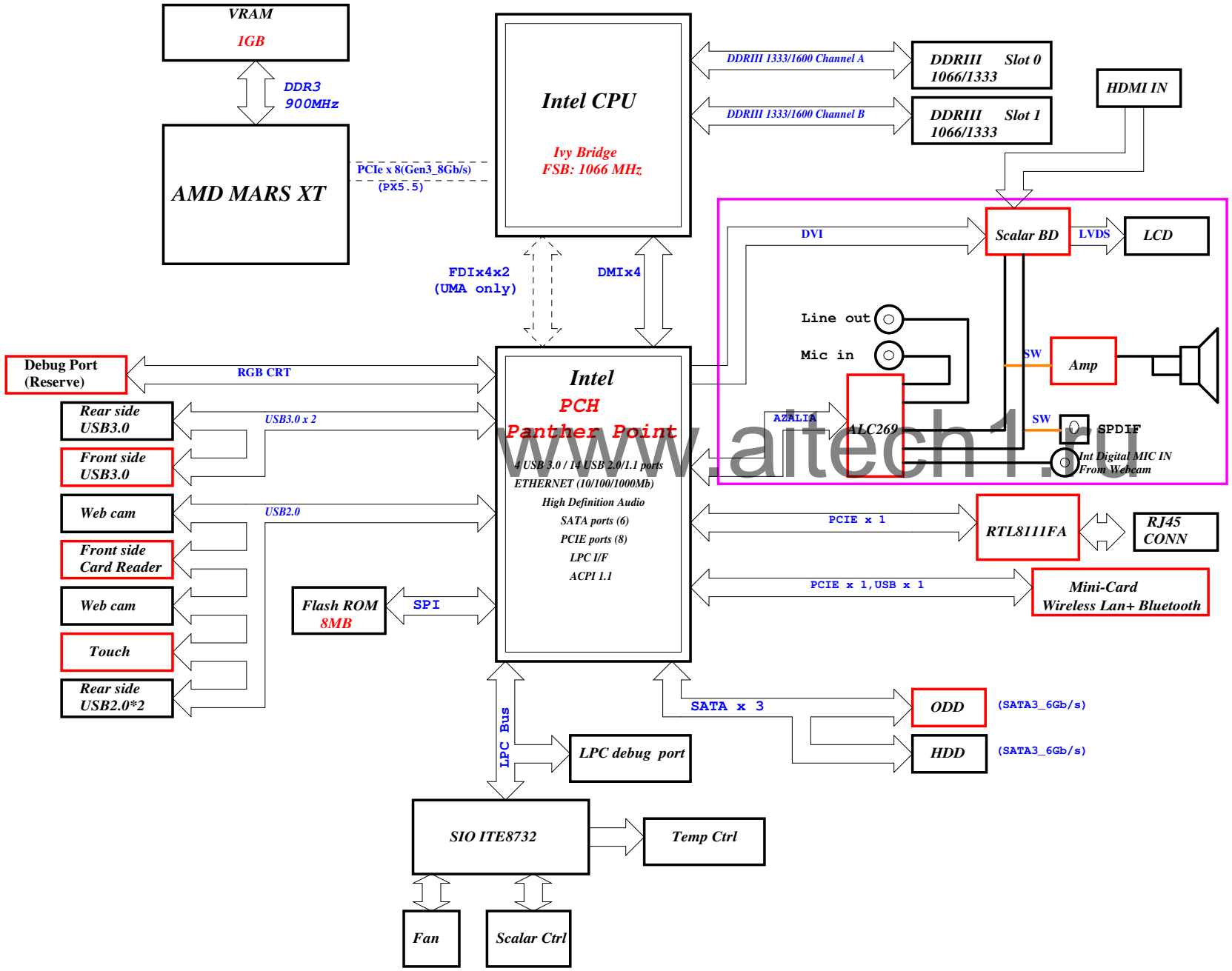
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 1 of 73

aPisa Block Diagram (UMA)

Project code :91.3KF01.001
PCB No :12074
Revision :SA
Project Name :PIM70L-aPisa 20



SYSTEM DC/DC RT8223MGQW	31
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_Charger 3D3V_A

CPU DC/DC ISL95832HRTZ	32~33
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95832HRTZ	34
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC ISL95870BHRZ	35
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51116RGER	36
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25PSP	37
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC TPS51461RGER	38
INPUTS	OUTPUTS
5V_S5	0D85V_S0

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

<Core Design>

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Title: BLOCK DIAGRAM
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 2 of 73

PCH Strapping Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

<Core Design>

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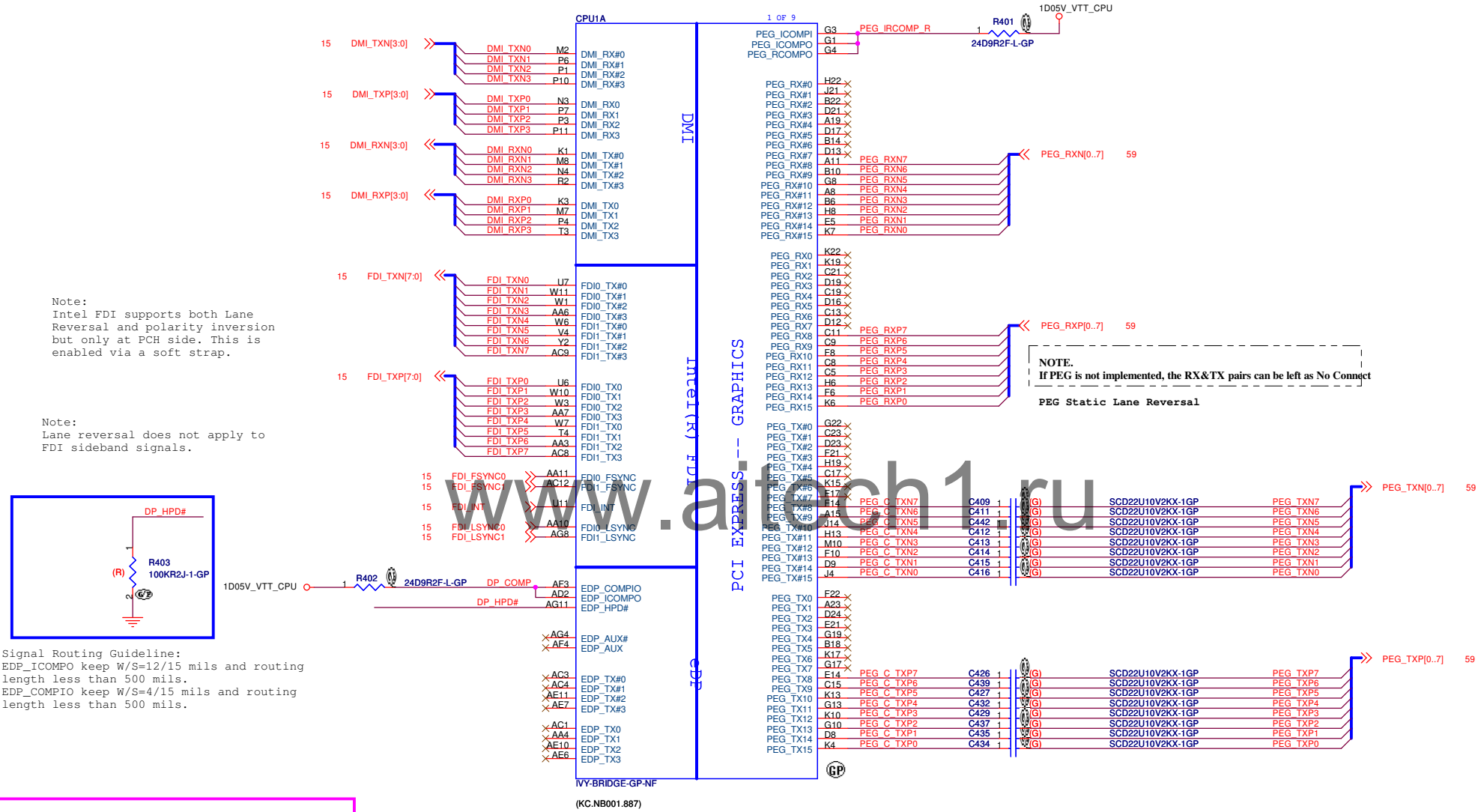
Title: Table of Content

Size: A3 | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 3 of 73

SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

1D05V_VTT_CPU — R402 24D9R2F-L-GP — DP_COMP

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

<Core Design>

Wistron Corporation
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Title: CPU (PCIE/DMI/FDI)
Size: A3 | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 4 of 73

SSID = CPU

CPU1B

2 OF 9

MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

1D05V_VTT_CPU

R501 62R2J-GP (63.75034.1DL)

H_PROCHOT#

C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

20121007 Charles Marge material

Connect EC to PROCHOT# through inverting OD buffer.

18 H_SNB_IVB# F49 PROC_SELECT#

JE40 modify C57 PROC_DETECT#

JE40 modify C49 CATERR#

18,52 H_PECI A48 PECI

29,32 H_PROCHOT# R513 56R2J-4-GP (63.47034.1DL) H_PROCHOT# R C45 PROCHOT#

20121007 Charles Marge material

18 H_THERMTRIP# D45 THERMTRIP#

Michael 2012/01/16

For EMI

H_CPUPWRGD C503 SCD1U16V2ZY-2GP

15 H_PM_SYNC C48 PM_SYNC

R503 10KR2J-3-GP

8 H_CPUPWRGD B46 UNCOREPWRGOOD

28 VDDPWRGOOD BE45 SM_DRAMPWROK

BUF_CPU_RST# C504 SCD1U16V2ZY-2GP

BUF_CPU_RST# D44 RESET#

3D3V_S0

RN503 SRN1K5J-1-GP

XDP_DBRESET#

14,51,52 PLT_RST# BUF_CPU_RST#

(66.47236.089)

20121007 Charles Marge material

VY-BRIDGE-GP-NF (KC.NB001.887)

BCLK J3 CLK_EXP_P 16
BCLK# H2 CLK_EXP_N 16

SB:SWAP

DPLL_REF_CLK AG3 CLK_DP_P
DPLL_REF_CLK# AG1 CLK_DP_N

R79133 1KR2J-1-GP
R79134 1KR2J-1-GP

1D05V_VTT

CLK_DP_N CLK_DP_P 16

20121007 Charles Marge material

If motherboard only supports external graphics or if it supports Processor Graphics but without eDP:
Connect DPLL_REF_CLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_CLK# on Processor to VCCP through 1K +/- 5% resistor

SM_DRAMRST# AT30 R502 4K99R2F-L-GP SM_DRAMRST# 28

SM_RCOMP0 BF44 SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 BG43 SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 BF43 SM_RCOMP_2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PRDY# N53
PREQ# N55

JE40 modify

TCK L56
TMS L55
TRST# J58 XDP_TRST#

TDI M60
TDO L59 XDP_TDO

DBR# K58 XDP_DBRESET#

BPM#0 G58
BPM#1 E55
BPM#2 E59
BPM#3 G55
BPM#4 G59
BPM#5 H60
BPM#6 J59
BPM#7 J61

JE40 modify

1D05V_VTT_CPU

R79135 47R2J-2-GP
R79136 47R2J-2-GP

XDP_TDO
XDP_TRST#

20121007 Charles Marge material

<Core Design>

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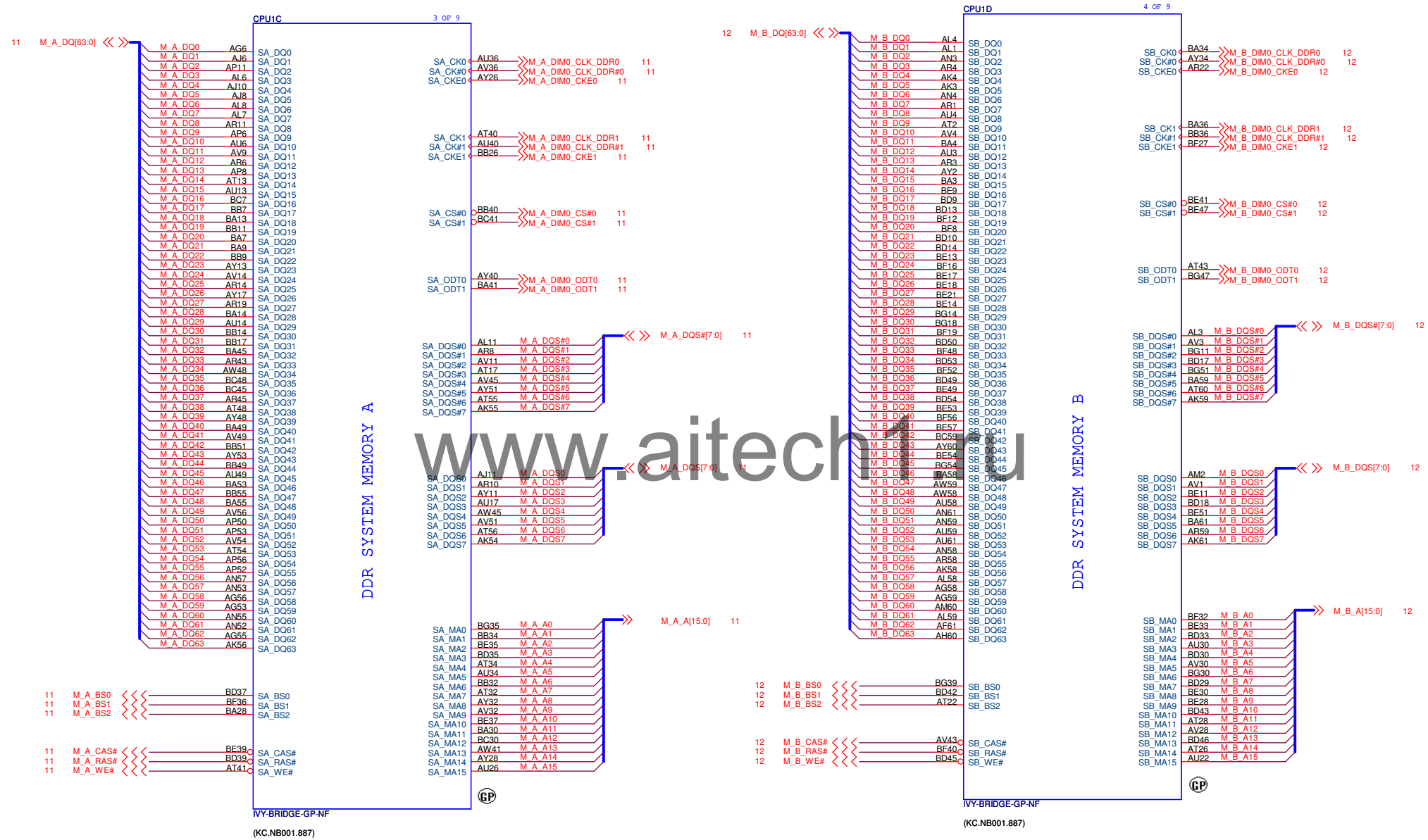
Title: CPU (THERMAL/CLOCK/PM)

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 5 of 73

SSID = CPU



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size: A3 | Document Number: aPISA | Rev: SA

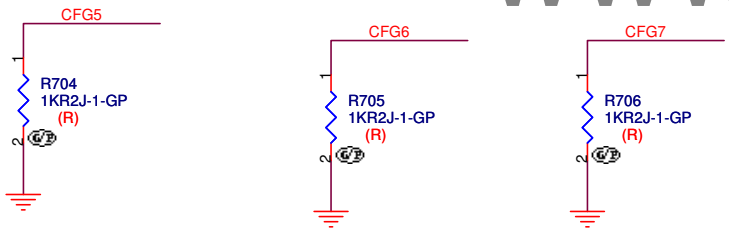
Date: Thursday, December 20, 2012 | Sheet 6 of 73

SSID = CPU

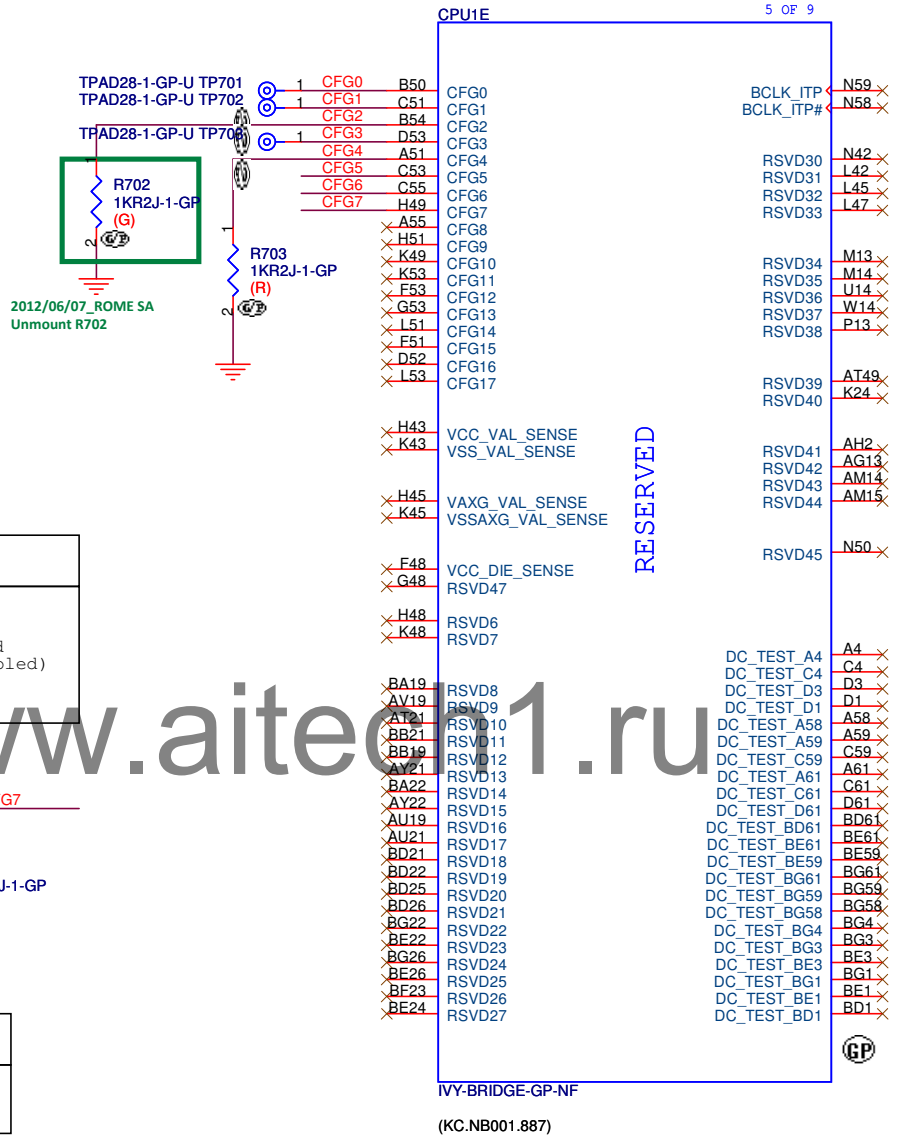
PEG Static Lane Reversal	
CFG2	PCI Express* Static x16 Lane Numbering Reversal. 1:Normal operation 0:Lane numbers Reversed

eDP Enable	
CFG4	1:Disable 0:Enable

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



<Core Design>

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Title: CPU (RESERVED)

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 7 of 73

SSID = CPU

PROCESSOR CORE POWER

33A

close to CPU

VCC_CORE

michael 2012/2/17 SB

POWER

CPU1F

6 OF 9

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF

(KC.NB001.887)

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
10 X 10UF
26 X 1UF

SB ADD

20121014 aPisa SB Charles
Change to Dip Cap

PIn BC22	1.05V_VTT
H	1.05V
L	1V

Michael 2012/01/16

According to intel comment

R810 Unmount

20121204 aPisa -1 Charles
0ohm short pad

Close to CPU

marge R usage Charles 20121007

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

R801,R802 close to CPU

<Core Design>

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 8 of 73

SSID = CPU

POWER

PROCESSOR VAXG: 24A

michael 2012/2/17 SB

michael 2012/2/17 SB

20121012 Jerry Modify

B4:VREF_DQ_CHA

D1:VREF_DQ CHB

Chief River

20121007 Charles change material

Iccmax:5A

20121012 Jerry Modify

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)

+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

R906,R907 close to CPU

PROCESSOR VCCPLL: 1.2A

R902 need be close to pin U10.

SB:must to be closed R902

20121016 aPisa SB Charles Change to Dip Cap

VCCSA Voltage Select

VID[1]	VID[0]	VCCSA
0	0	0.9 V
1	0	0.8 V
0	1	0.725 V
1	1	0.675 V

IVY-BRIDGE-GP-NF
(KC.NB001.887)

<Core Design>

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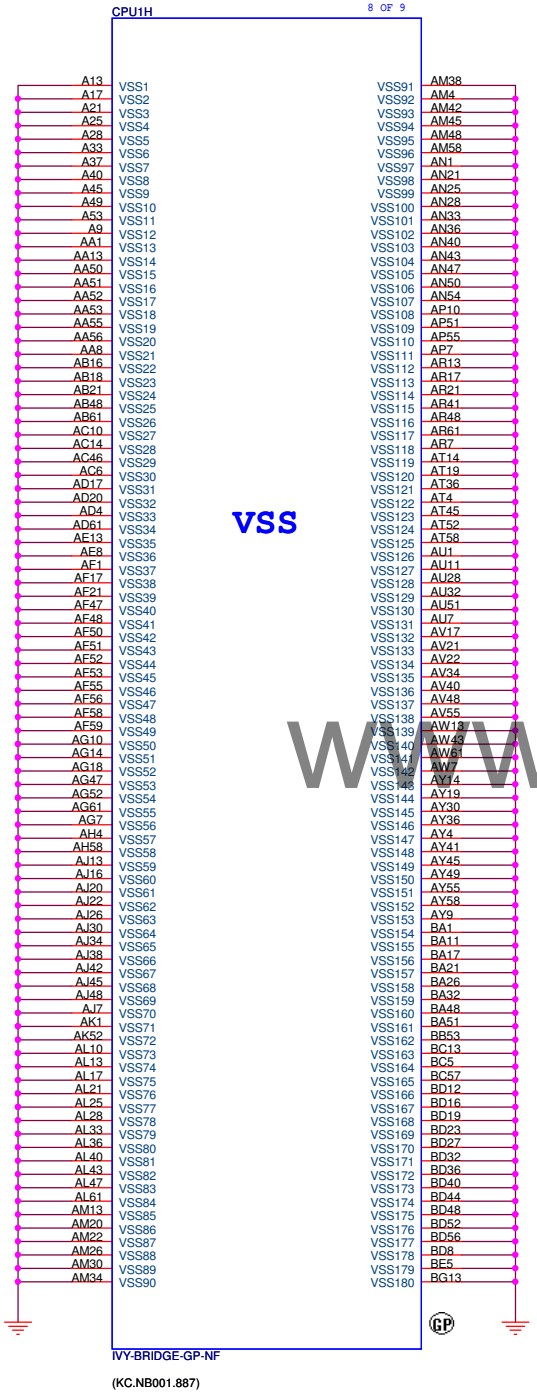
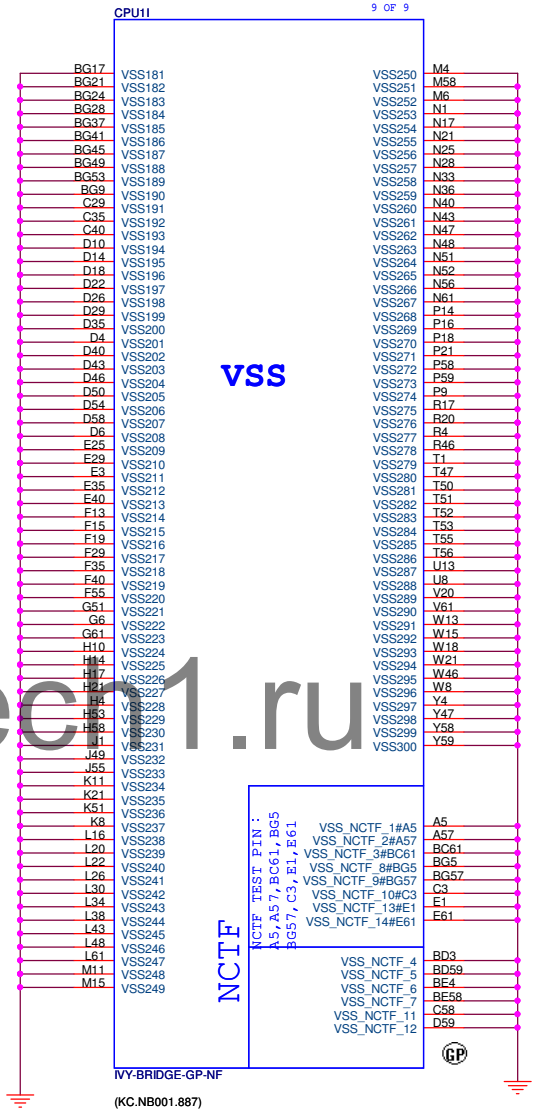
Title: CPU (VCC_GFXCORE)

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 9 of 73

SSID = CPU





<Core Design>

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Title: CPU (VSS)

Size: A3 | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 10 of 73

SSID = MEMORY

H = 5.2mm
(STD Type)

2011/9/30

change the P/N of DIMM SLOT

Done

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

DIMM1 (62.10024.P41)

M_A_A[15:0] 6

M_A_BS2 6
M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6

M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6

DDR3_DRAMRST# 2,28

M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6

M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6

M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6

M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6

M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6

SMB_DATA 12,16,25,49,56
SMB_CLK 12,16,25,49,56

TS#_DIMM0_1 12

DDR_WR_VREF01_B4 28

DDR3-204P-233-GP

Thermal EVENT

TS#_DIMM0_1 — R1403 10KR2J-3-GP — 3D3V_S0

DIMM VREF OP1

20121012 Jerry Modify

1D5V_S3

R153 1KR2F-3-GP
C540 SCD1U16V2ZY-2GP (R)
R154 1KR2F-3-GP
DIMM_DQ_VREF_A_L — R157 0R0402-PAD-1-GP — DIMM_DQ_VREF_A
C102 SCD1U10V2KX-4GP (78.10421.2FL)
20121204 aPisa -1 Charles
0ohm short pad
R158 0R0402-PAD-2-GP

R724 1KR2F-3-GP
C511 SCD1U16V2ZY-2GP (R)
R723 1KR2F-3-GP
DIMM_CA_VREF_A_L — R720 0R0402-PAD-1-GP — DIMM_CA_VREF_A
C505 SCD1U10V2KX-4GP (78.10421.2FL)

−2

Place these caps close to VTT1 and VTT2.

0D75V_S0
C1419 SC1U6D3V2KX-GP
C1421 SC1U6D3V2KX-GP

20121012 Jerry Modify

SODIMM A DECOUPLING

1D5V_S3
C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 (R) SC10U10V5ZY-1GP
C1406 SC10U6D3V5KX-1GP
C1416 SCD1U10V2KX-5GP
C1417 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

<Core Design>

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Title: DDR3-SODIMM1
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 11 of 73

SSID = MEMORY

H = 5.2mm
(Reverse Type)

20121012 Jerry
Modify

DIMM VREF OP1

2011/9/30

change the P/N of DIMM SLOT

Done

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

DIMM2 (62.10024.P51)

DDR3-204P-234-GP

20121204 aPisa -1 Charles
0ohm short pad

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

-2

Place these caps close to VTT1 and VTT2.

20121012 Jerry
Modify

<Core Design>

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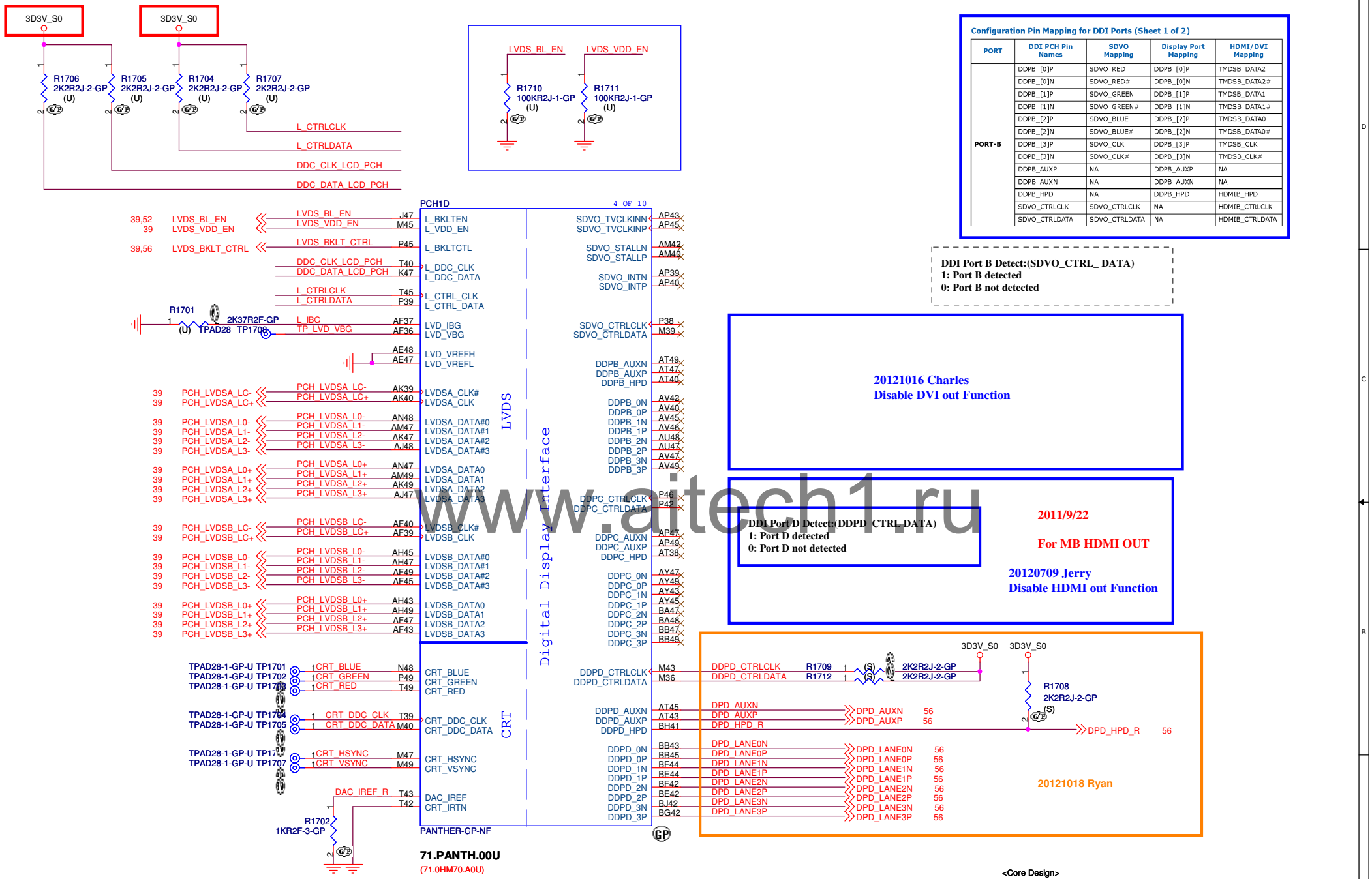
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 12 of 73



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)				
PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

DDI Port B Detect:(SDVO_CTRL_ DATA)
1: Port B detected
0: Port B not detected

20121016 Charles
Disable DVI out Function

DDI Port D Detect:(DDPD_CTRL_DATA)
1: Port D detected
0: Port D not detected

2011/9/22

For MB HDMI OUT

20120709 Jerry
Disable HDMI out Function

20121018 Ryan

71.PANTH.00U
(71.0HM70.A0U)

<Core Design>

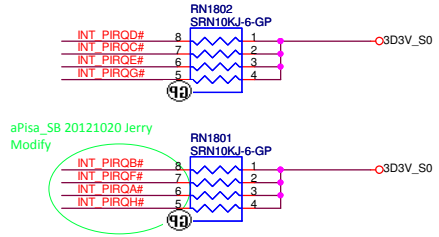
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 13 of 73

SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

Debug Port device (DPD) must be high-speed capable and connect directly to Port 1 and Port 9 on PCH-based systems (such as, the DPD cannot be connected to Port 1/Port 9 through a hub. When a DPD is detected the PCH EHCI will bypass the integrated Rate Matching Hub and connect directly to the port and the DPD.).

	Express Chipset
Total number of USB ports	8[8]
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)	2[9]
• USB 2.0 Only Ports	6

8. USB ports 4, 5, 6,7,12 and 13 are disabled on 8 port SKUs.
9. USB 3.0 ports 3 and 4 are disabled on 2 SuperSpeed port-capable SKUs.

Debug Port device (DPD) must be high-speed capable and connect directly to Port 1 and Port 9 on PCH-based systems (such as, the DPD cannot be connected to Port 1/Port 9 through a hub. When a DPD is detected the PCH EHCI will bypass the integrated Rate Matching Hub and connect directly to the port and the DPD.).

USB Table

2011/10/12

Pair	Device
0	Front USB3.0 Ext. port 2
1	USB3.0 Ext. port 1
2	Touch
3	Front CR
4	X
5	X
6	X
7	X
8	Ext. USB2.0
9	Ext. USB2.0
10	Bluetooth
11	Webcam
12	X
13	X

2011/11/22
Add for rear USB overcurrent protection

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

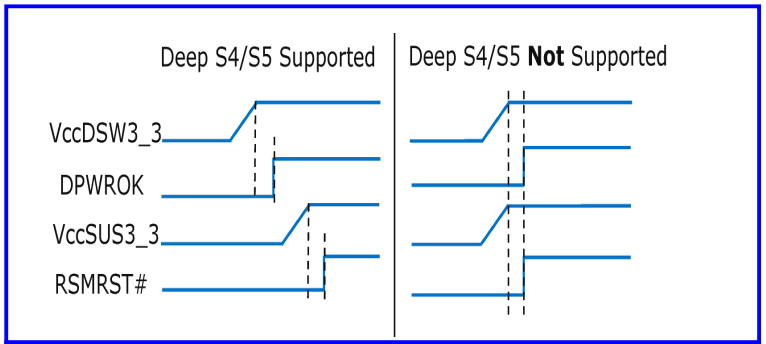
Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: aPISA | Rev: SA

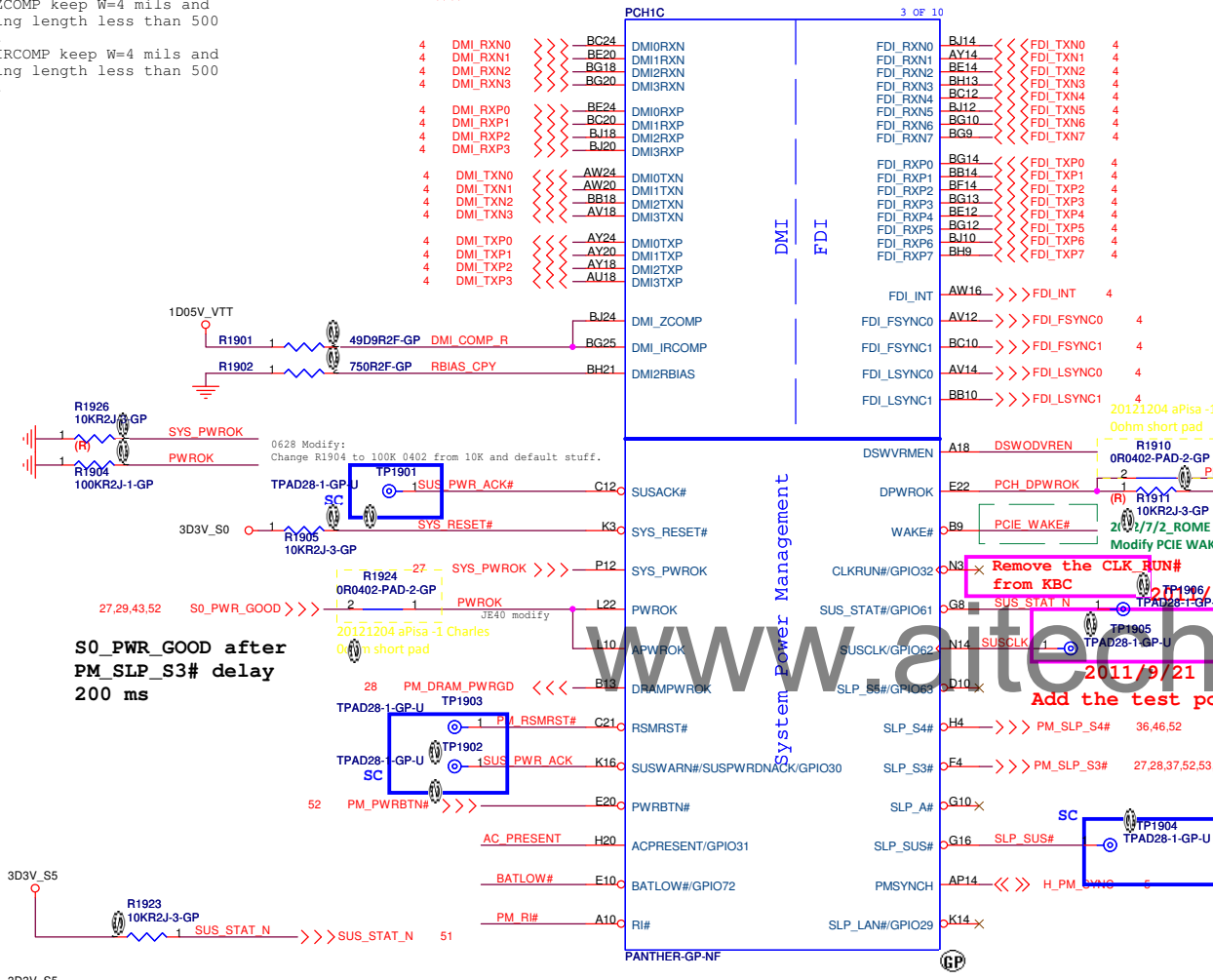
Date: Thursday, December 20, 2012 | Sheet 14 of 73

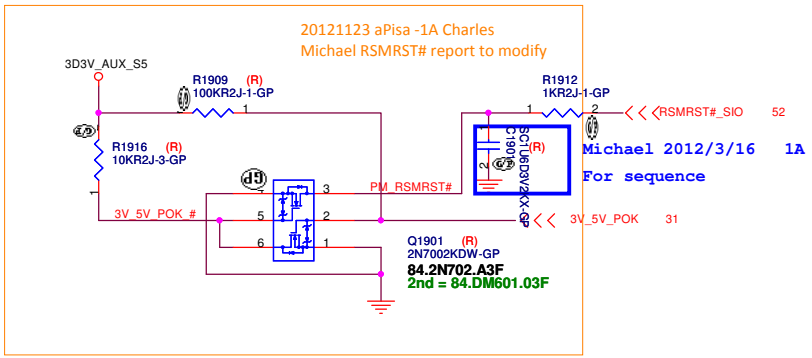
SSID = PCH

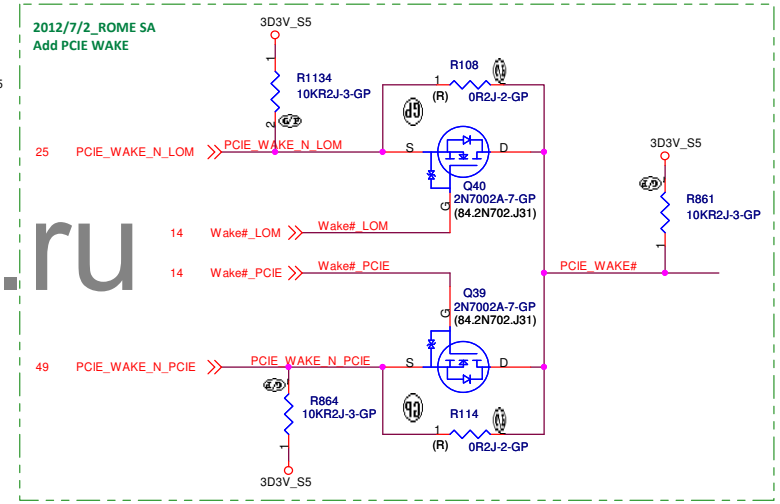
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



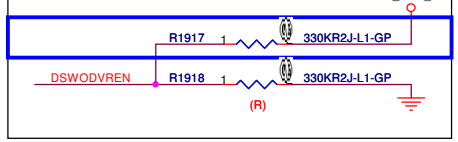
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30







DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 15 of 73

SSID = PCH

2012/5/23_ROME SA
Delete TV Tuner

2012/5/23_ROME SA
Delete TV Tuner

2011/9/21
Connect to SIO PME, refer to Zappa

Michael 2012/02/10 SB

For DIS_PX mode or MXM mode.

Michael 2012/02/13 SB

CRB : 1K
CEKLT: 10K

R2008 and C2008 CO-LAY

2011/9/22

Need to check the value about this resistor
Add the R2008 for SIO 48MHZ

Michael 2011/01/16
For EMI

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

need very close to PCH

<Core Design>

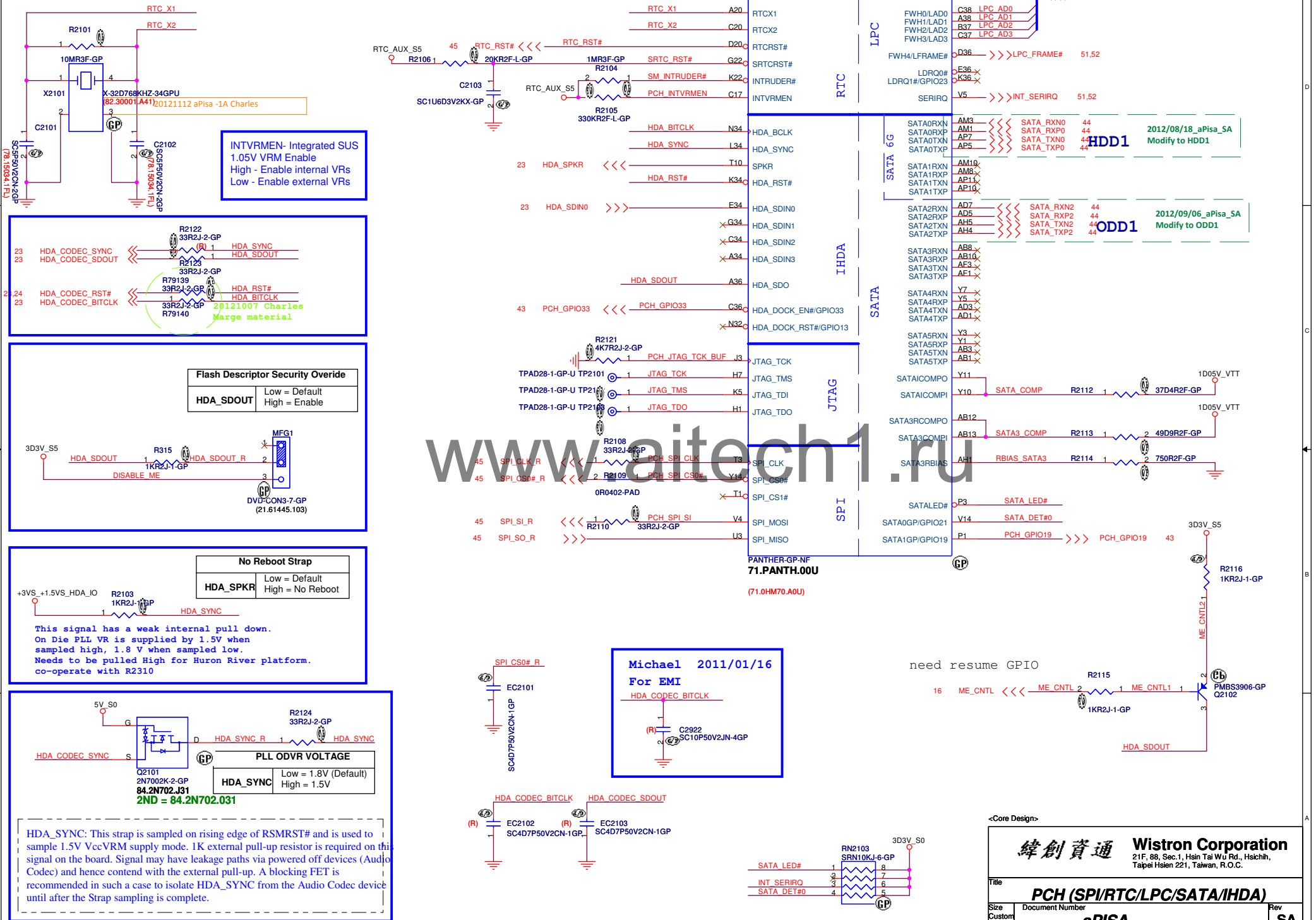
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: Custom | Document Number: aPISA | Rev: SA

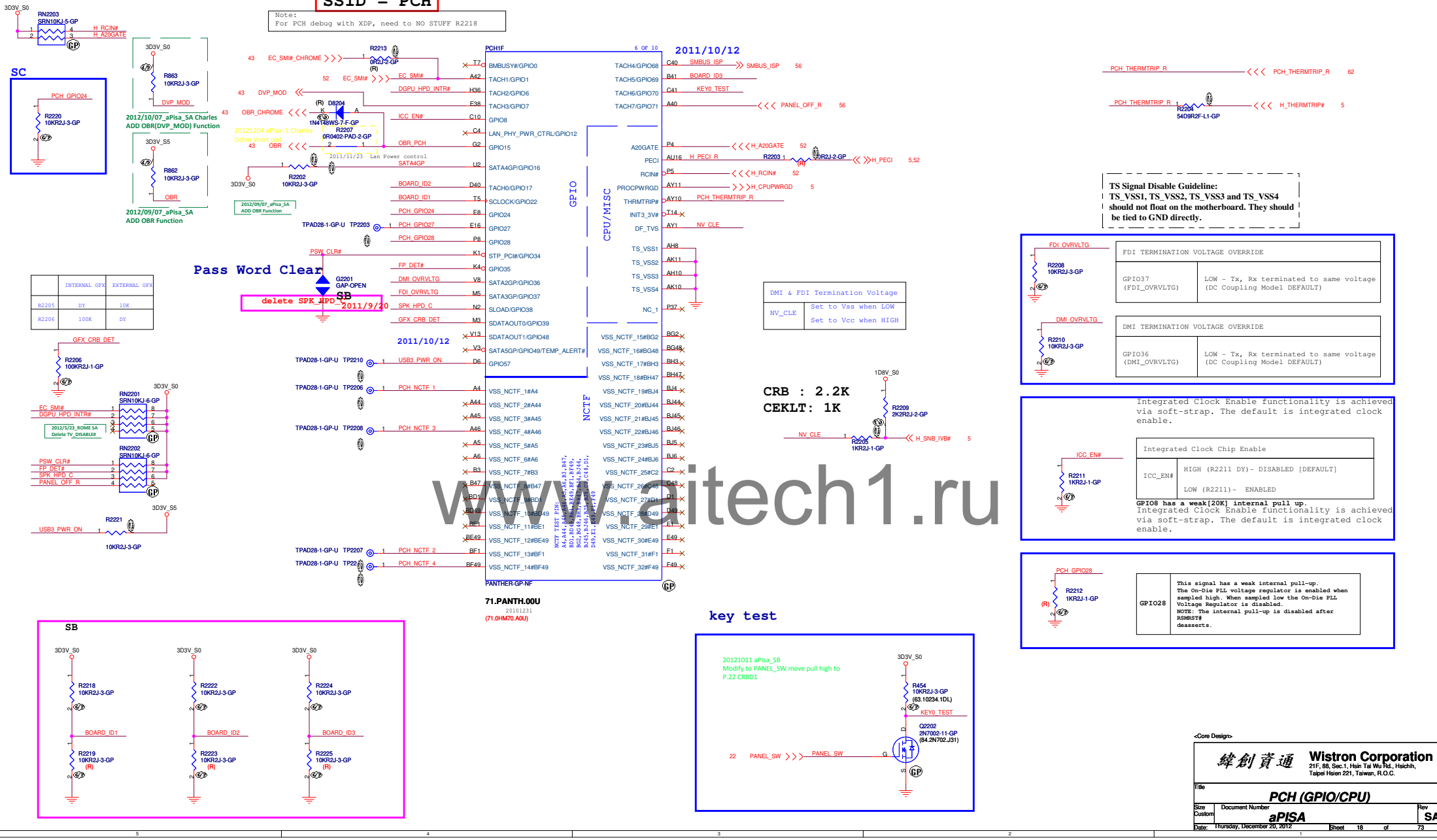
Date: Thursday, December 20, 2012 | Sheet 16 of 73

SSID = PCH

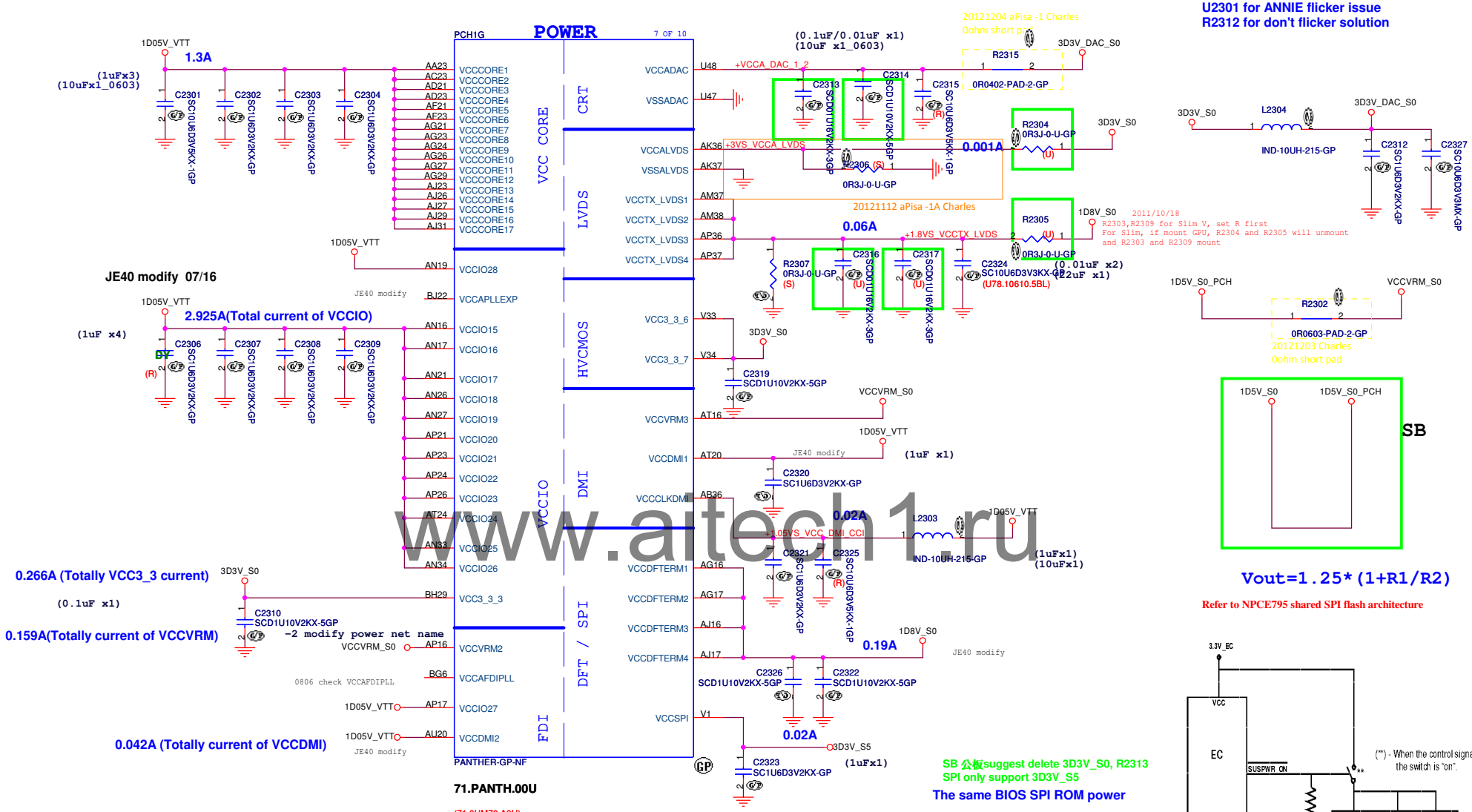


SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218



SSID = PCH 6A



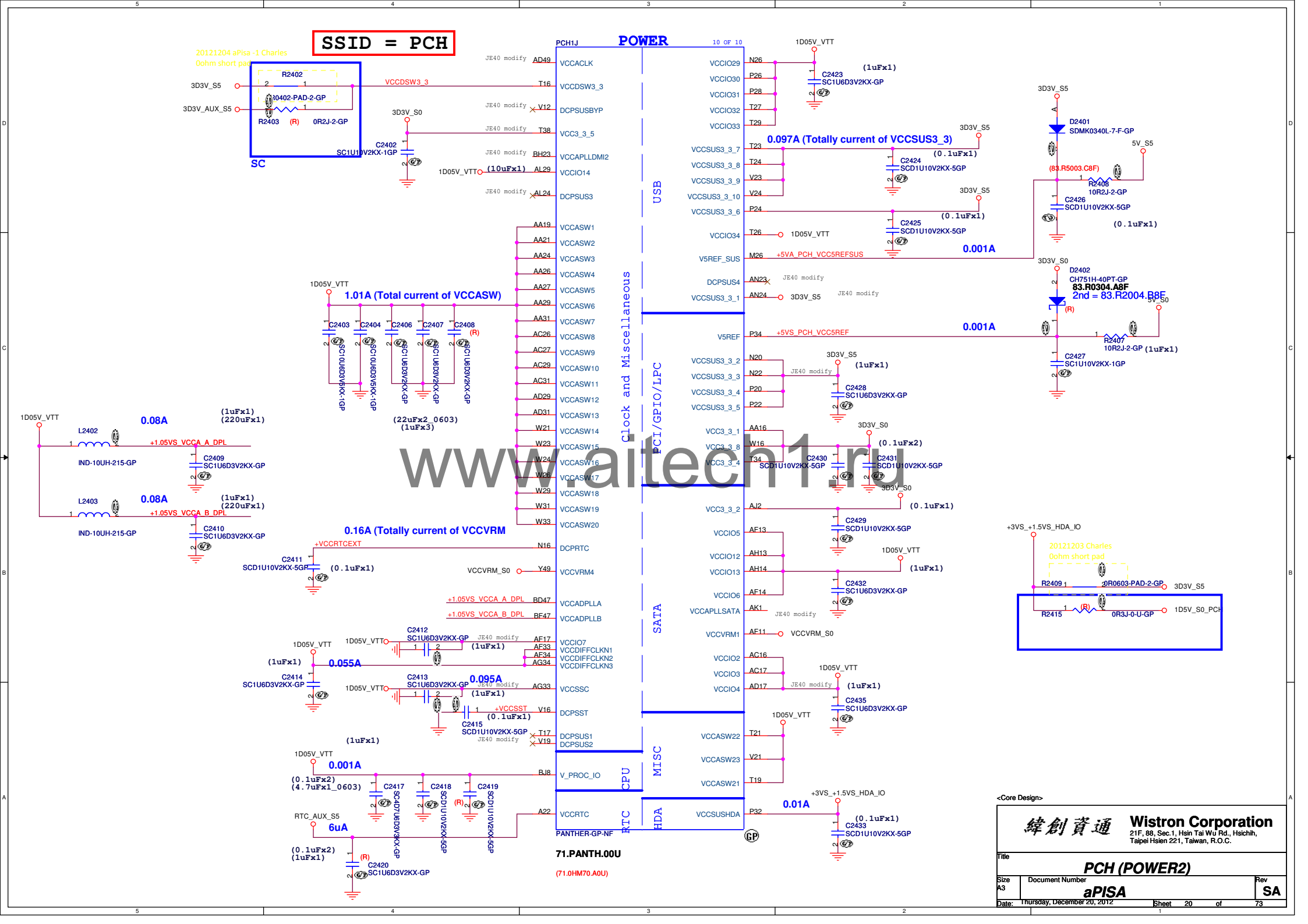
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

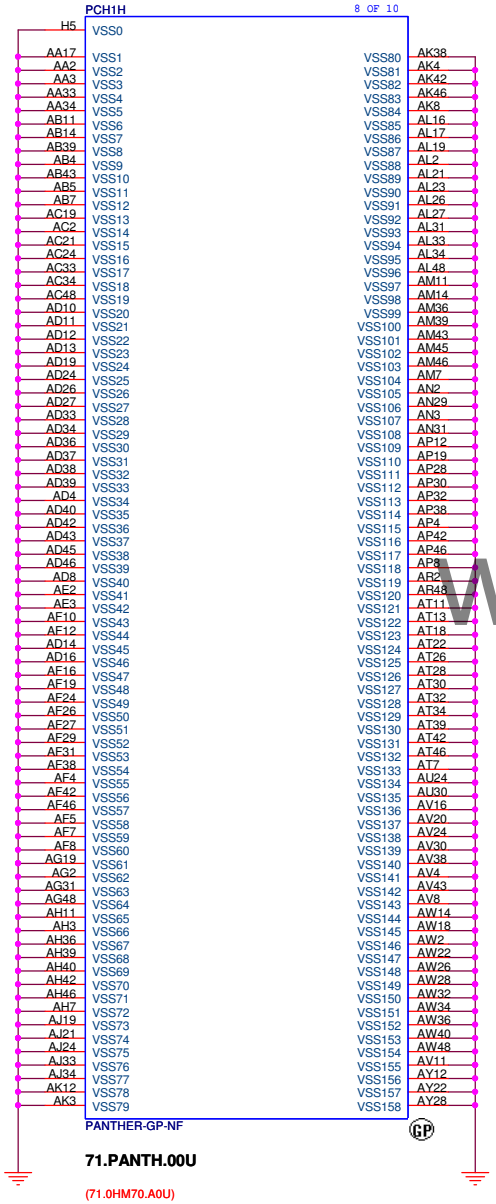
Title: PCH (POWER1)

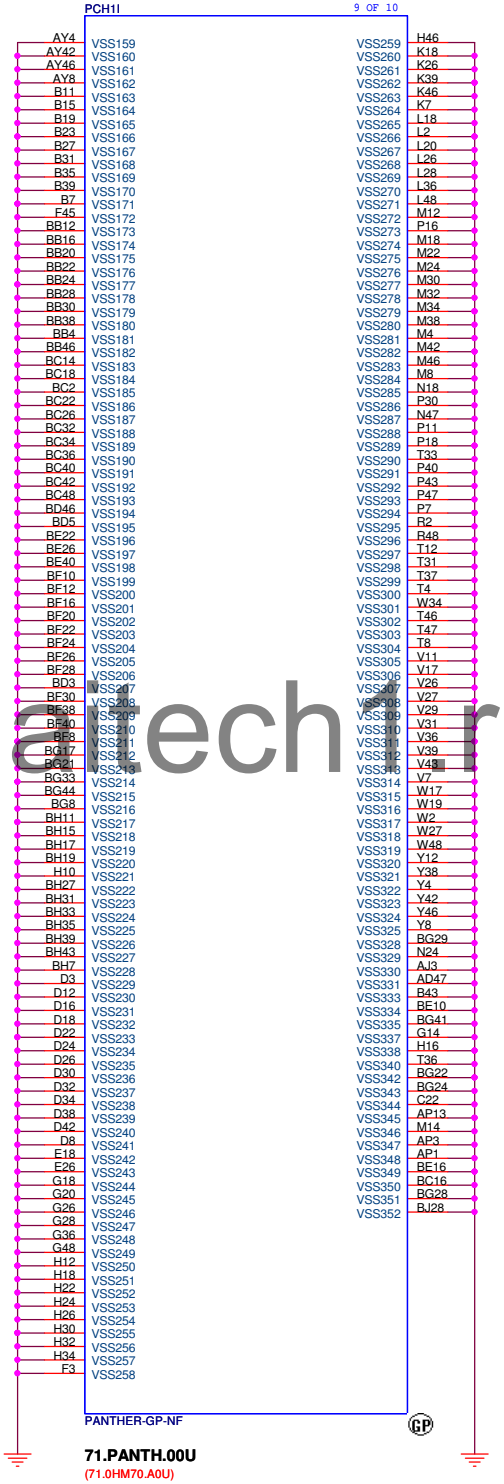
Size: A3 | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 19 of 73



SSID = PCH





<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size	Document Number	Rev
A3	aPISA	SA

Date: Thursday, December 20, 2012 Sheet 21 of 73

2012/09/04_aPisa_SA
Delete USB3.0 Power

USB3.0 CONNECTORFROM Co-lay

2012/08/18_aPisa_SA
Delete USB3.0 Connector

2012/09/10_aPisa_SA
ADD EMC protect

20121112 aPisa -1A Charles
moune com-choke for card-reader USB2.0

L6307 MCM1012B900FBP-GP-U
L6308 MCM1012B900FBP-GP-U
20121021 Jerry
Marge material

if change 0ohm use (66.R0036.04L)

2012/08/24_aPisa_SA
ADD AUBD1 connector

AUBD1
close to AUBD1 as much as possible.
MIC_IN_CON
Combo_C
L9517 MHC1608S601LBP-GP
HP_OUT_R_CON
HP_OUT_L_CON
JD_HP_C
L9518 MHC1608S601LBP-GP
JWT-CON8-21-GP (20.F1819.008)
20121206 Charles
Add EMI solution
AGND

20121205 Charles
Add EMI solution
near to AUBD1 two side
close to AUBD1 as much as possible.
DCBATOUT
EC9715 SC100P50V2JN-3GP
EC9716 SC100P50V2JN-3GP
C9658 SC100P50V2JN-3GP
C9657 SC100P50V2JN-3GP
AGND

MB/DB side Audio Connector			
Pin	Net		Note
1	Audio_GND	GND	
2	MIC	O	analog
3	MIC Verf	O	analog
4	Audio_GND	GND	
5	Line out_R	O	analog
6	Line out_L	O	analog
7	Line out_JD	I	analog
8	Audio_GND	GND	

A channel is RX , B channel is TX

U9605
PS8713BTQFN24GTR2-A0-1-GP
20121203 aPisa -1 Charles
un-mount & short Wire for signal trace
UnMount for SB
Charles 20121019

2012/07/10
USB3.0 Redriver

2012/07/12
If use NXP
R112,R118= 0ohm
R80=NC

If use TI
R112,R118,R80= 0ohm

20121013_aPisa_SB Charles
Modify

2012/08/24_aPisa_SA
Modify Pin define

20121016 aPisa SB Charles
Mount panel on/off EC control only W/O Scalar

20121112 aPisa -1A Charles
Change to solve leacke

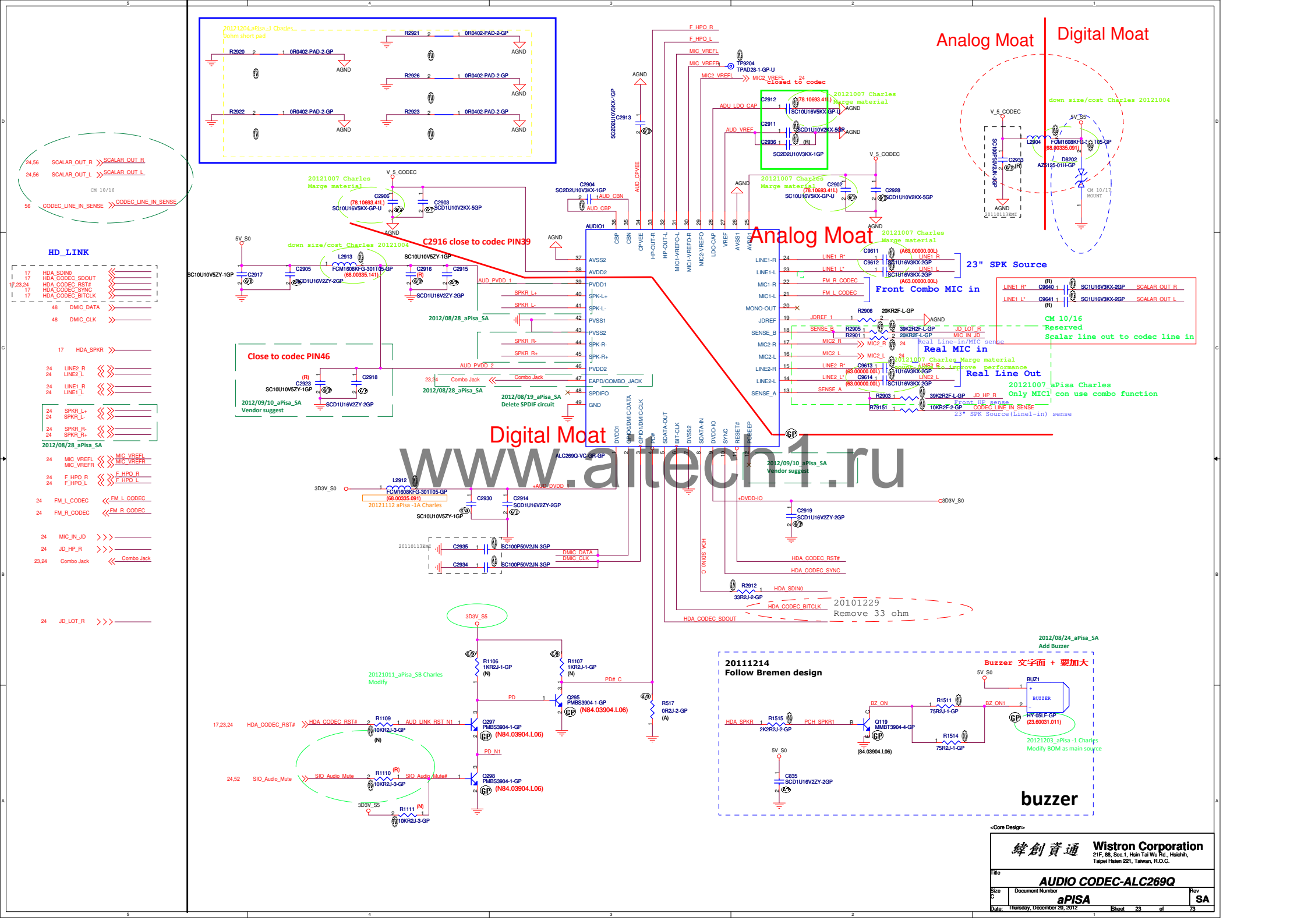
CRBD1
ACES-CON26-17-GP-U (20.K0767.026)

MB 26Pin cconnector Pin define			
Pin	Net		Note
1	GND	GND	
2	USB 3V	I/O	card reader
3	USB 3V	I/O	card reader
4	GND	GND	
5	Switch	I/O	panel on/off
6	GND	GND	
7	USB2.0 D+ #1	I/O	card reader
8	USB2.0 D- #1	I/O	card reader
9	GND	GND	
10	GND	GND	
11	USB3.0 TX+ #1	I/O	USB3.0
12	USB3.0 TX- #1	I/O	USB3.0
13	GND	GND	
14	USB2.0 D- #1	I/O	USB3.0
15	USB2.0 D+ #1	I/O	USB3.0
16	GND	GND	
17	USB3.0 RX+ #1	I/O	USB3.0
18	USB3.0 RX- #1	I/O	USB3.0
19	GND	GND	
20	GND	GND	
21	USB 5V	I/O	USB3.0
22	USB 5V	I/O	USB3.0
23	GND	GND	
24	GND	GND	
25	reserve		
26	reserve		

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

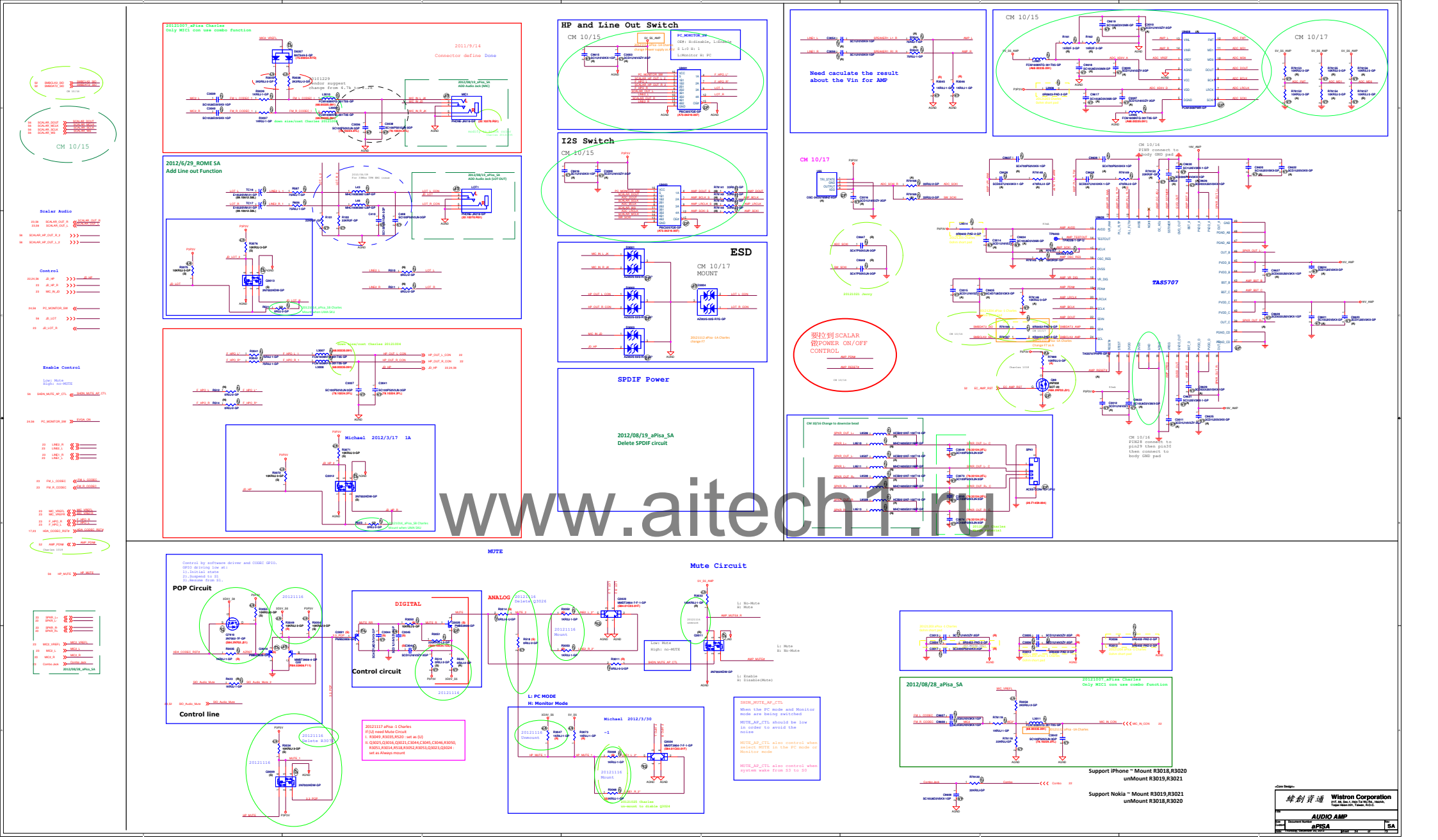
Title: Front BD Connector
Size: A3 | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 22 of 73

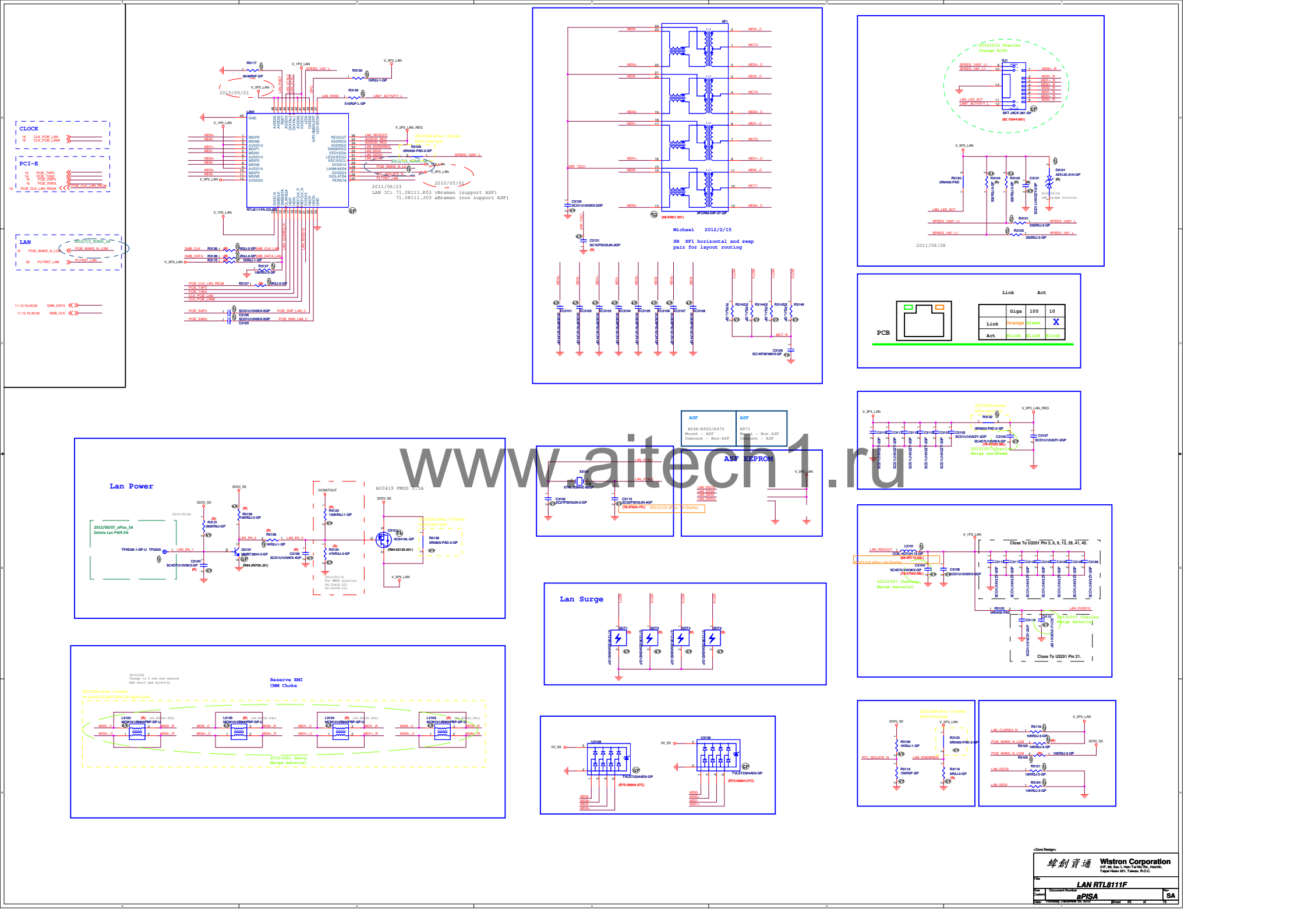


Title: AUDIO CODEC-ALC269Q

Size	Document Number	Rev
C	aPISA	SA

Date: Thursday, December 20, 2012 Sheet 23 of 73





(SD, SDHC, MMC, MS, MS_Pro, XD)

2012/07/12 Jerry
Card reader move to small board

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5138 (CARD READER)

Size: Custom | Document Number: aPISA | Rev: SA

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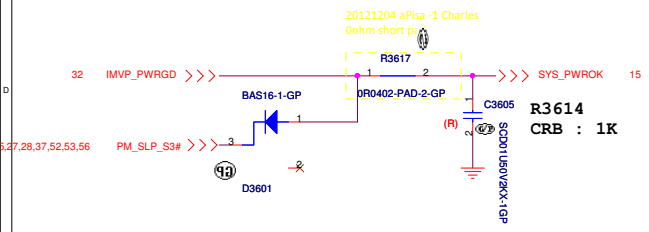
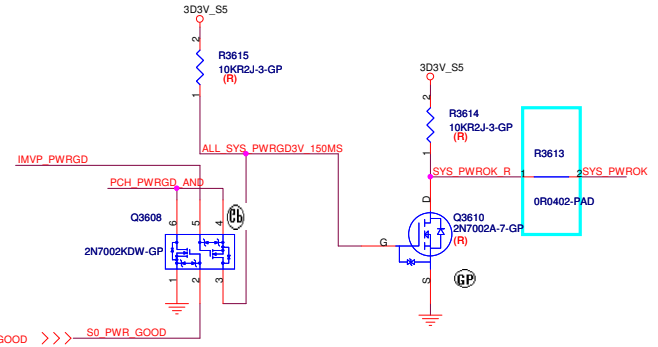
Power Sequence

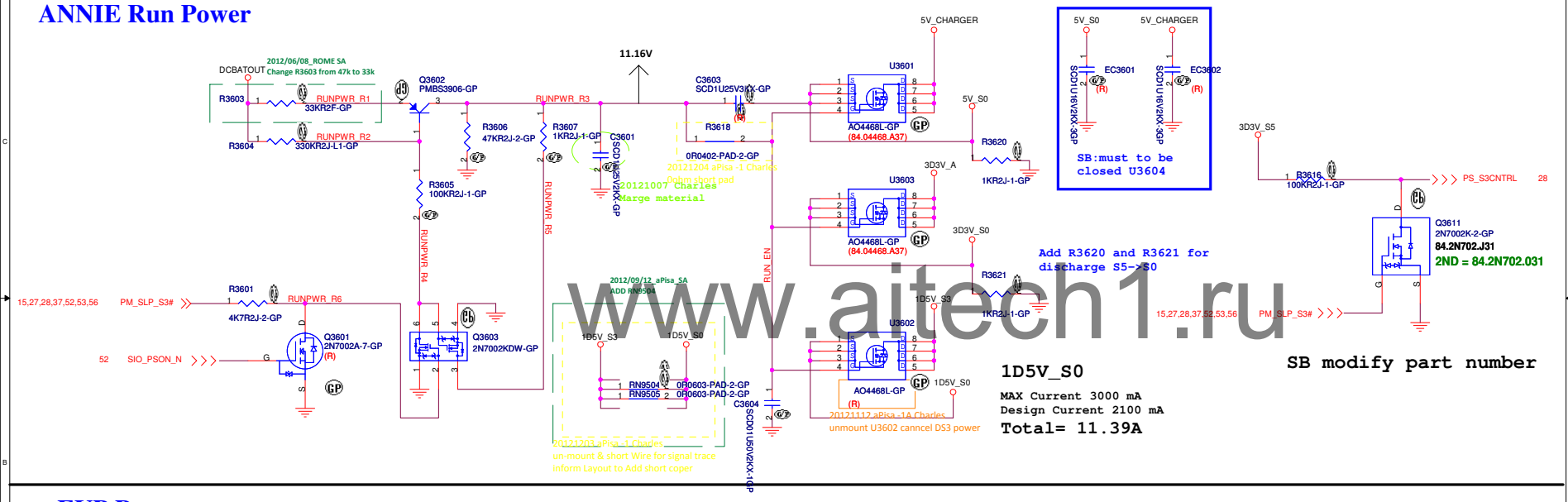




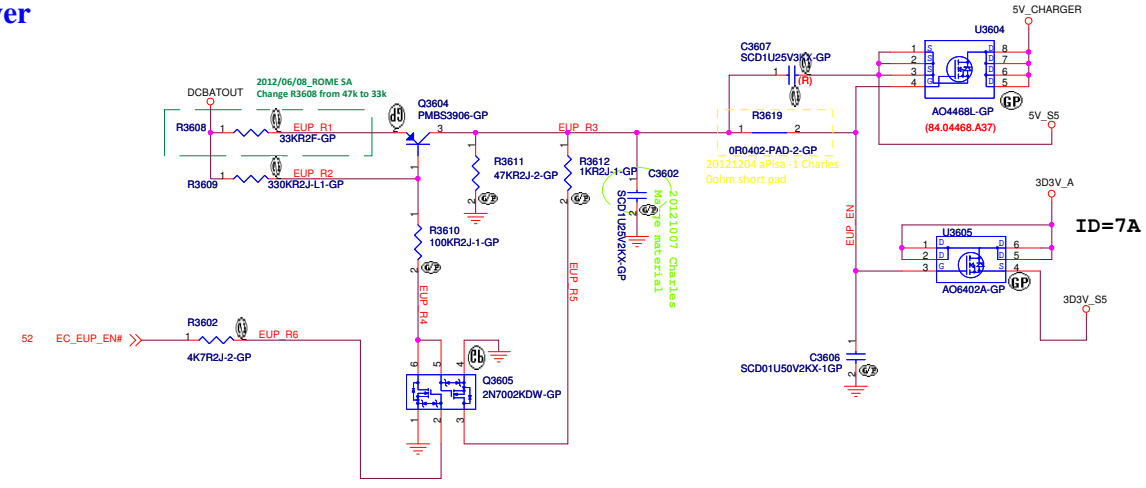
2011/9/22

Reserve for system power ok

ANNIE Run Power



EUP Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER & SEQUENCE**

Size	Document Number	Rev
Custom	aPISA	SA

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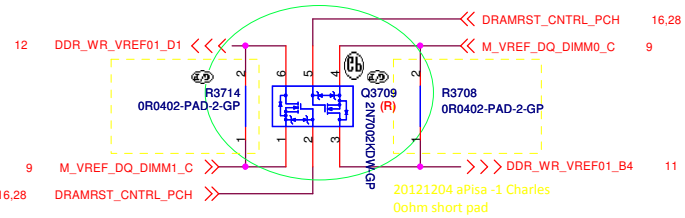
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

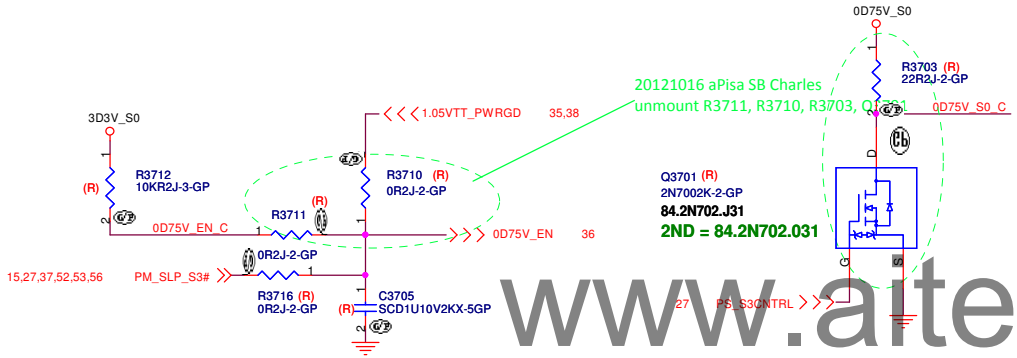
20121012 Jerry
Delete

⑤ S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

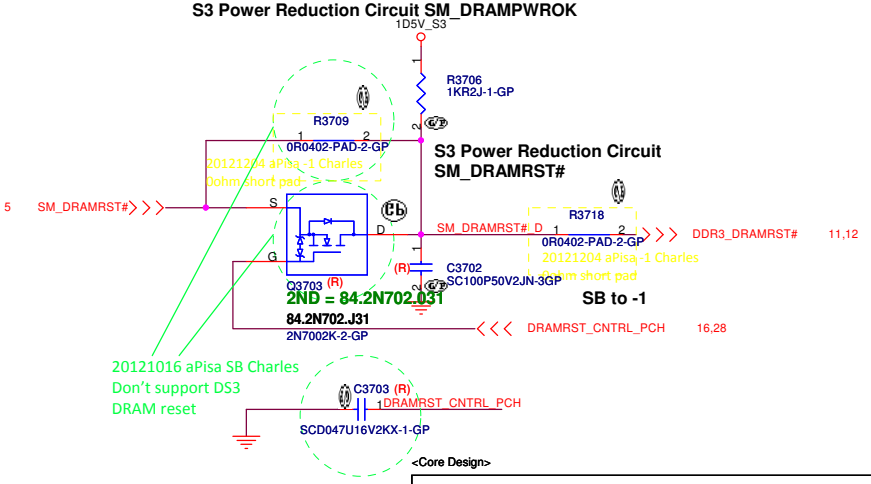
20121016_aPisa_SB Charles
modify DIMM VREF



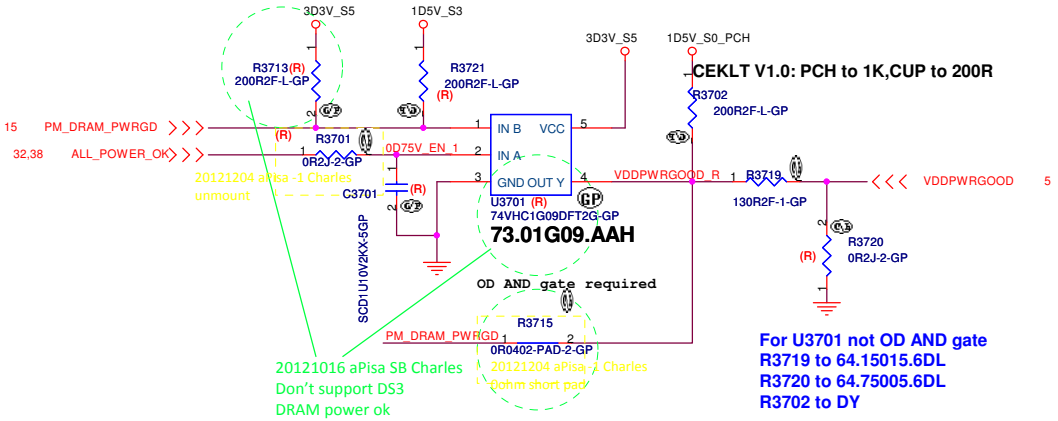
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SB
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER OCP / S3 reduction
Size: A3 | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 28 of 73

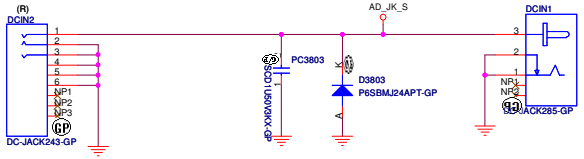
ANNIE solution

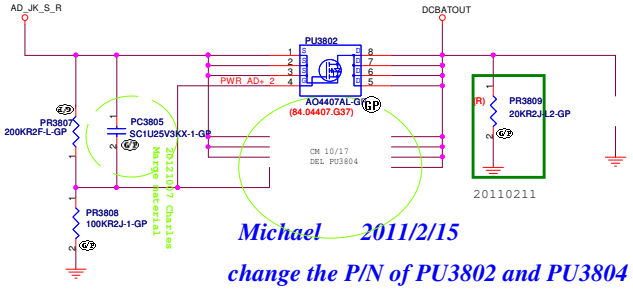
Michael 2011/12/12

Remove Power connector about aNice
Remain DC IN Jack

2011/9/19
change AD+ to DCBATOUT

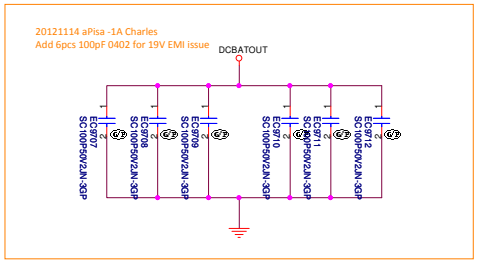
20121016_aPisa_SB Charles
Add F7 (O) for OCP solution





Michael 2011/2/15

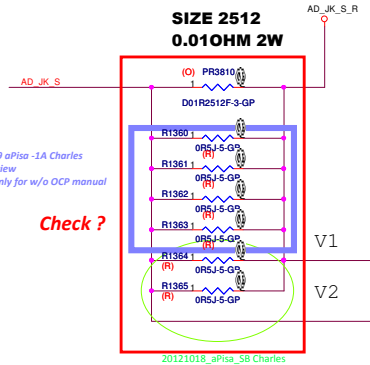
change the P/N of PU3802 and PU3804



SIZE 2512
0.01OHM 2W

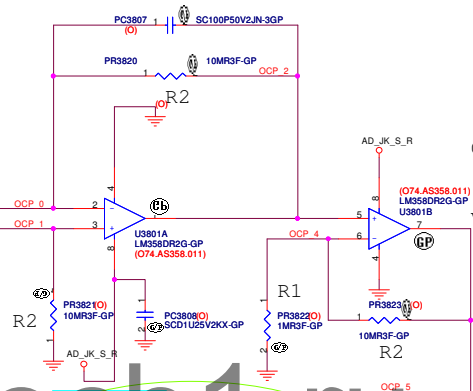
20121119 aPisa -1A Charles
BOM Review
Mount Only for w/o OCP manual

Check ?



GAIN1= VO/(V2-V1)=R2/R1

20110209



GAIN2= 1+R2/R1

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN JACK
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 29 of 73

2012/08/18_aPisa_SA

Delete BATT CONN

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A4	aPISA	SA

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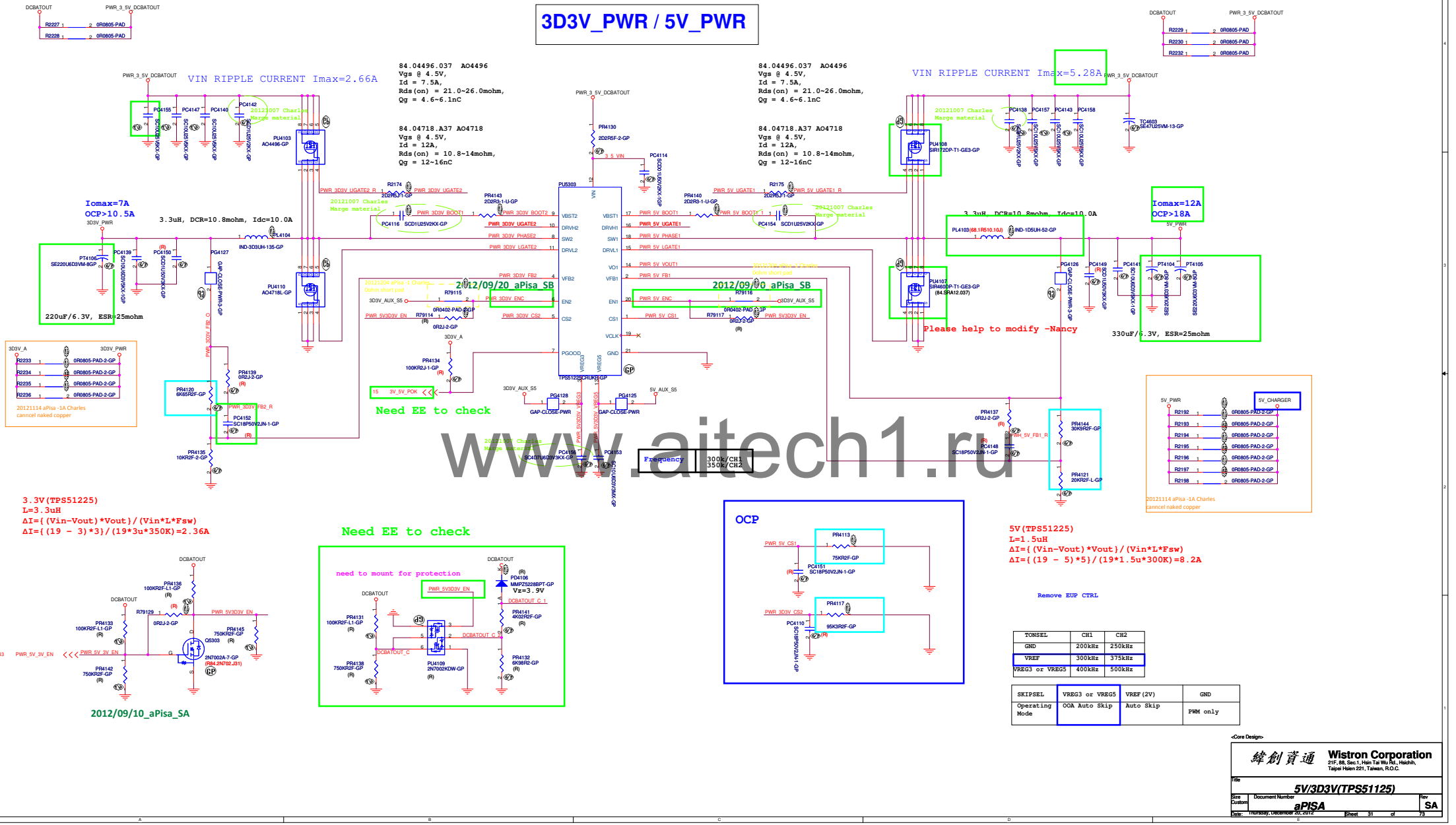
3D3V_PWR / 5V_PWR

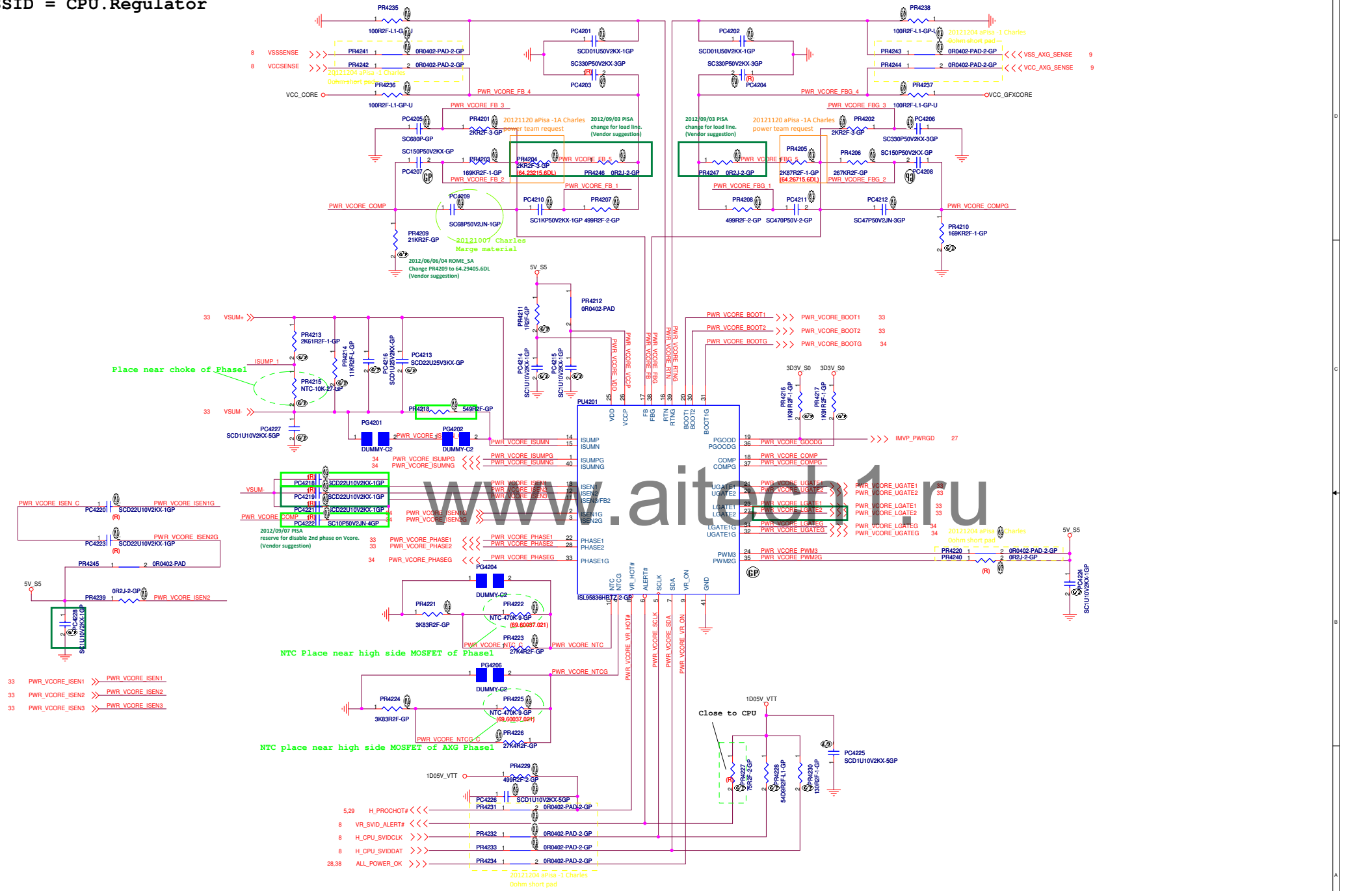


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

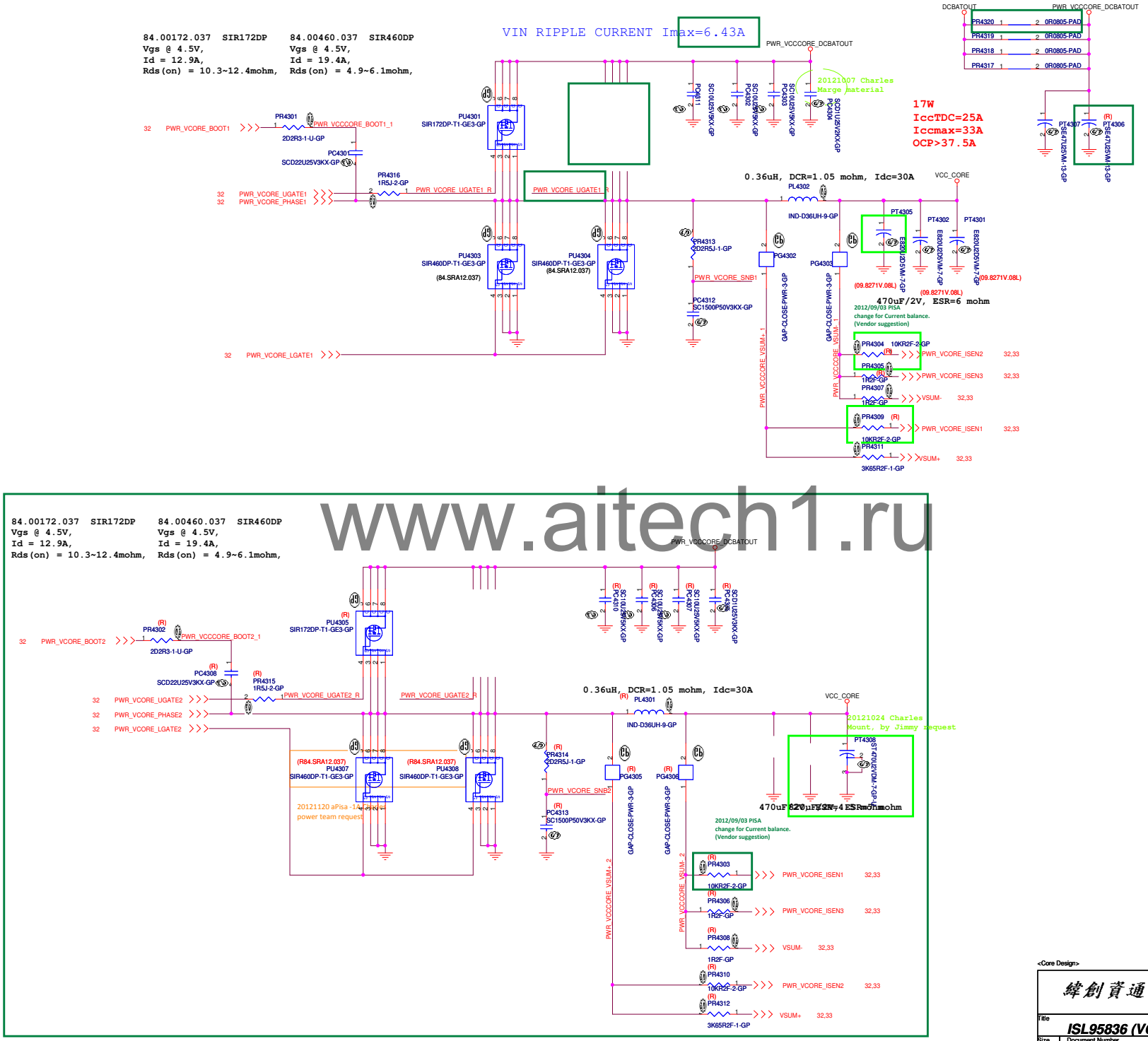
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: 5V/3D3V(TPS51125)
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 31 of 73

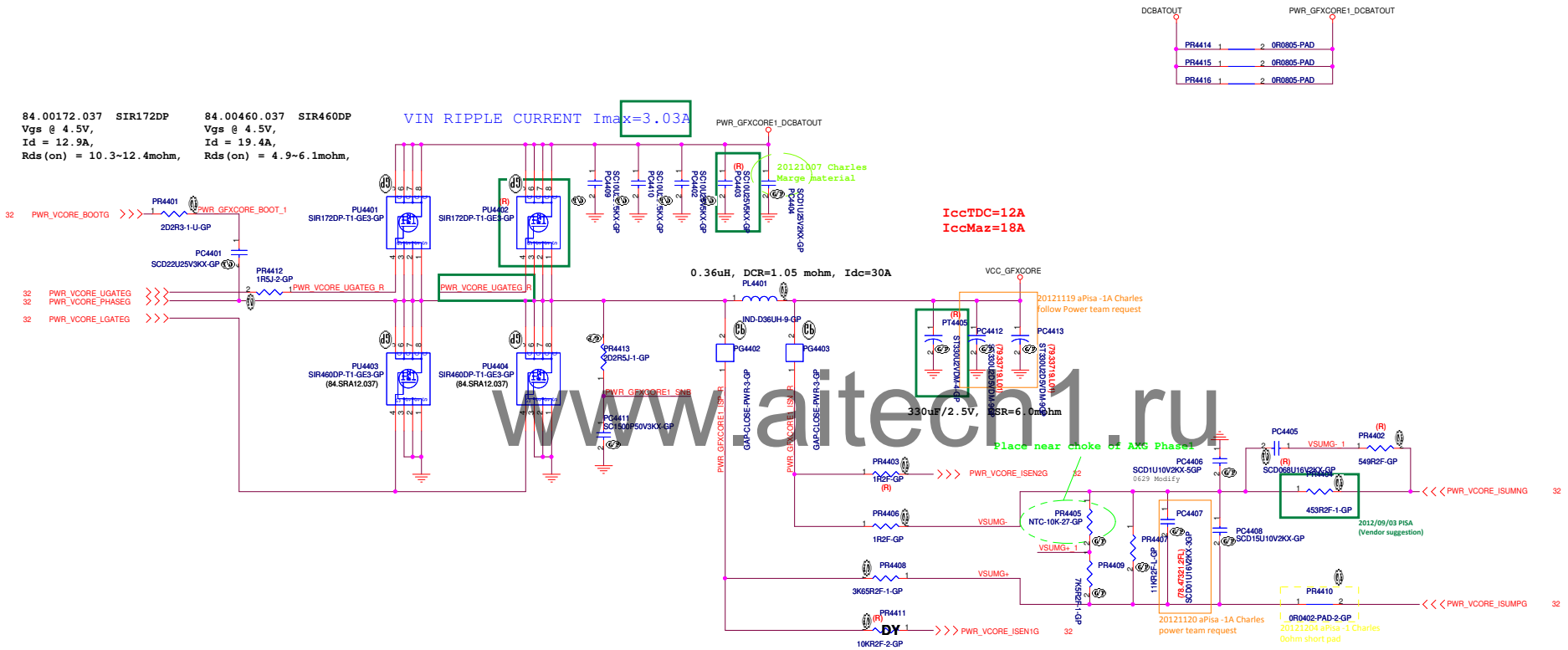
SSID = CPU.Regulator



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL95836 (VRM)
Size: C	Document Number: aPISA
Rev	SA
Date: Thursday, December 20, 2012	Sheet 32 of


84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 10.3~12.4mohm,
84.00460.037 SIR460DP
Vgs @ 4.5V,
Id = 19.4A,
Rds(on) = 4.9~6.1mohm,
VIN RIPPLE CURRENT Imax=6.43A
PWR_VCCCORE_DCBATOUT
DCBATOUT
20121107 Charles
Marge material
17W
IccTDC=25A
Iccmax=33A
OCP>37.5A
0.36uH, DCR=1.05 mohm, Idc=30A
VCC_CORE
470uF/2V, ESR=6 mohm
2012/09/03 PISA
change for Current balance.
(Vendor suggestion)
PWR_VCORE_BOOT1
PWR_VCCCORE_BOOT1_1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_VCORE_LGATE1
PWR_VCORE_UGATE1_R
PWR_VCORE_SNB1
PWR_VCCCORE_VSUM+_1
PWR_VCCCORE_VSUM-_1
PWR_VCORE_ISEN2
PWR_VCORE_ISEN3
PWR_VCORE_ISEN1
VSUM-
VSUM+
IND-D36UH-9-GP
GAP-CLOSE-PWR-3GP
PU4301 SIR172DP-T1-GE3-GP
PU4303 SIR460DP-T1-GE3-GP
PU4304 SIR460DP-T1-GE3-GP
(84.SRA12.037)
84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 10.3~12.4mohm,
84.00460.037 SIR460DP
Vgs @ 4.5V,
Id = 19.4A,
Rds(on) = 4.9~6.1mohm,
PWR_VCCCORE_DCBATOUT
0.36uH, DCR=1.05 mohm, Idc=30A
VCC_CORE
20121024 Charles
Mount, by Jimmy Request
20121120 aPisa -14
power team request
2012/09/03 PISA
change for Current balance.
(Vendor suggestion)
PWR_VCORE_BOOT2
PWR_VCCCORE_BOOT2_1
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_VCORE_LGATE2
PWR_VCORE_UGATE2_R
PWR_VCORE_SNB2
PWR_VCCCORE_VSUM+_2
PWR_VCCCORE_VSUM-_2
PWR_VCORE_ISEN1
PWR_VCORE_ISEN3
PWR_VCORE_ISEN2
VSUM-
VSUM+
IND-D36UH-9-GP
GAP-CLOSE-PWR-3GP
PU4305 SIR172DP-T1-GE3-GP
PU4307 SIR460DP-T1-GE3-GP
PU4308 SIR460DP-T1-GE3-GP
(R84.SRA12.037)
www.aitech1.ru
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL95836 (VCORE)
Size C
Document Number
aPISA
Rev SA
Date: Thursday, December 20, 2012
Sheet 33 of



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

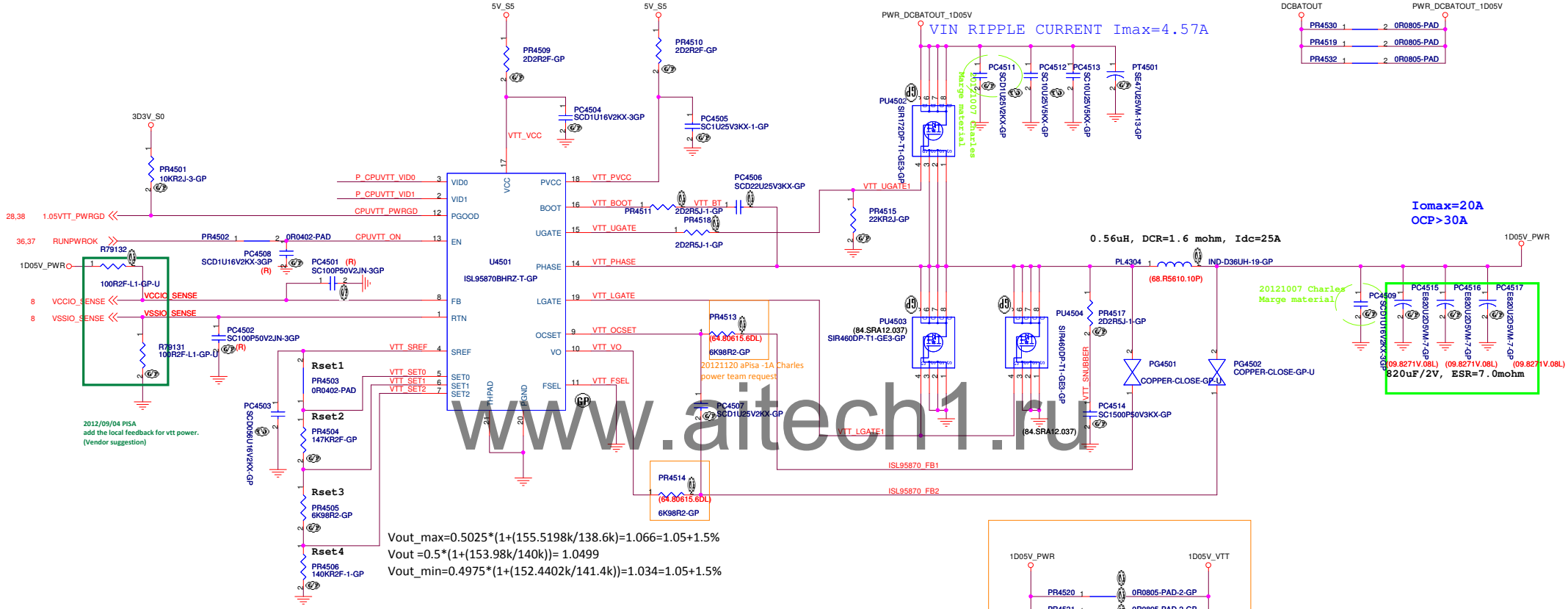
Title: ISL95836 (VCC_GFXCORE)

Size: C | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 34 of

84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 10.3~12.4mohm,

84.00460.037 SIR460DP
Vgs @ 4.5V,
Id = 19.4A,
Rds(on) = 4.9~6.1mohm,

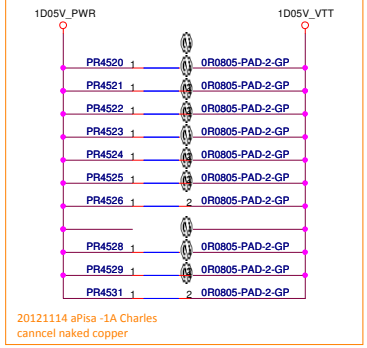


Vout_max=0.5025*(1+(155.5198k/138.6k)=1.066=1.05+1.5%
Vout =0.5*(1+(153.98k/140k))= 1.0499
Vout_min=0.4975*(1+(152.4402k/141.4k))=1.034=1.05+1.5%

PR4507 10KR2F-2-GP P_CPUVTT_VID0
PR4508 10KR2F-2-GP P_CPUVTT_VID1

VID0	VID1	Vout
0	0	1.05V

FIX at 1.05V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D05V(ISL95870B)
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 35 of 73

SSID = PWR.Plane.Regulator_1p5v0p75v

TPS51211 for 1D5V

1.5V_DDR

VIN RIPPLE CURRENT Imax=5.4A

84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 12.9A,
Rds(on) = 10.3~12.4mohm,

84.00460.037 SIR460DP
Vgs @ 4.5V,
Id = 19.4A,
Rds(on) = 4.9~6.1mohm,

0.68uH, DCR=2.4mohm, Idc=22A

Iomax=20A
OCP>30A

330uF/2.5V, ESR=9.0mohm

VOUT=((R1+R2)/R2)*0.7

Need EE to check

OCP setting

PWM Frequency setting

20121120 aPisa -1A Charles power team request

20121007 Charles Marge material

20121114 aPisa -1A Charles canncel naked copper

APL5337 for 0D75V

V_SM_VTT

DDR3_MEM_VTT
0D75V

+0.75VS
Iomax: 1.0A

PD Internally Limit
(125'c - 25'c)/55 =1.82W

PD=(Vin-Vout)*Iomax
=(1.5-0.75)*1A=0.75W

Iomax=1.0A

Need EE to check

20121203 aPisa -1 Charles 0ohm short pad

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

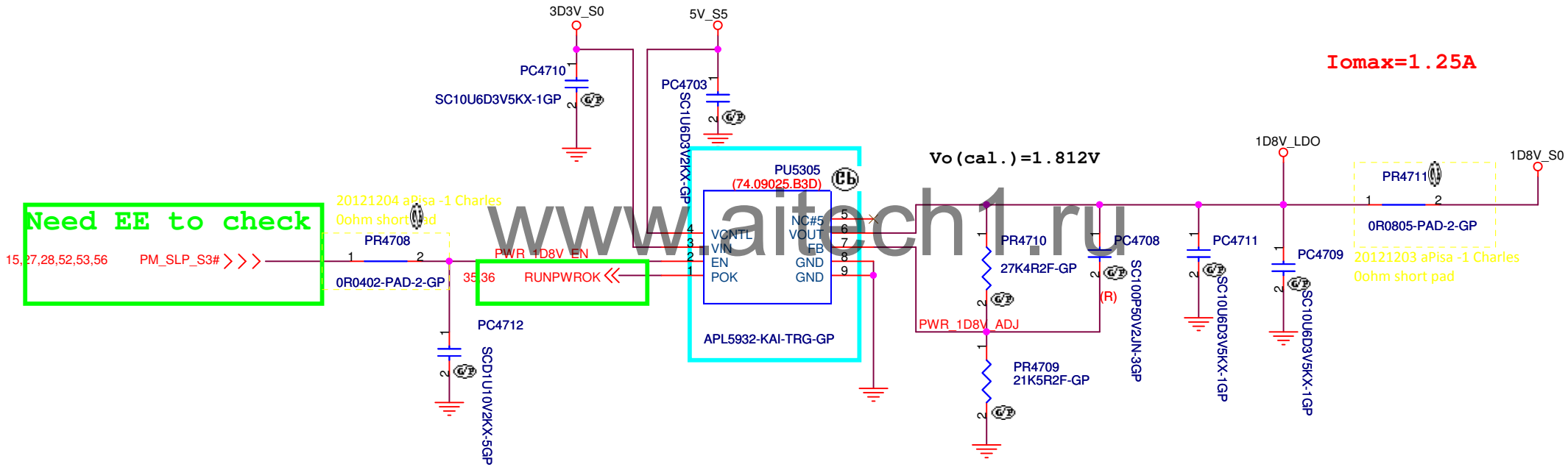
Title: DDR 1D5V & 0D75V (TPS51211)

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 36 of 73

SSID = PWR.Plane.Regulator_1p8v

APL5932 for 1D8V_S0

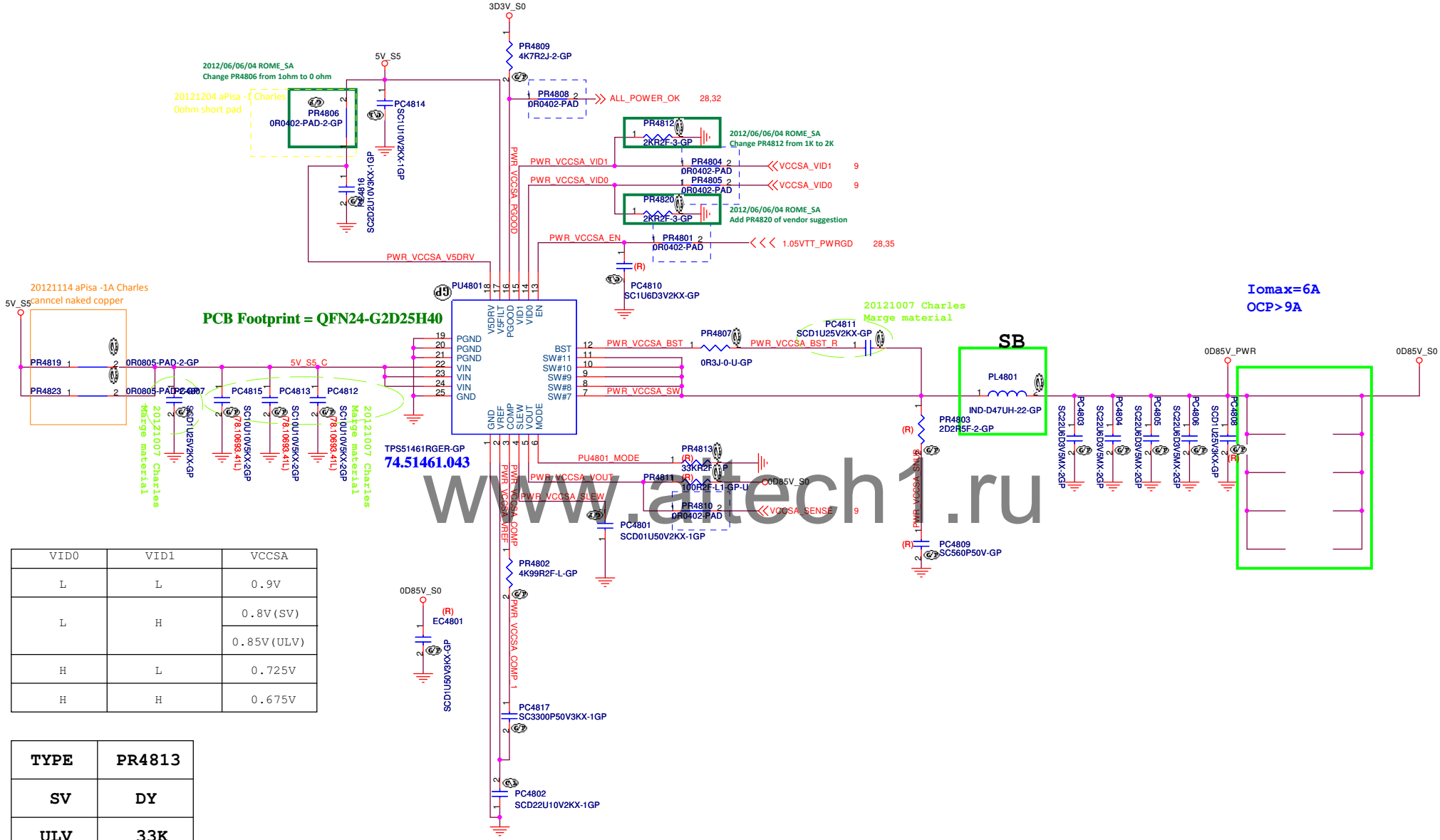


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D8V_LDO(APL5932)	
Size: Custom	Document Number: aPISA	Rev: SA
Date: Thursday, December 20, 2012	Sheet 37 of 73	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V(SV)
		0.85V(ULV)
H	L	0.725V
H	H	0.675V

TYPE	PR4813
SV	DY
ULV	33K

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: VCCSA (TPS51461)

Size: A3 | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 38 of 73

SSID = VIDEO

+19V_S5_INV Power

2012/08/23_aPisa_SA

For UMA
Low: Disable
High: Enable

For Scalar
Low: Enable
High: Disable

68.00216.191
Z=80 ohm,Rdc=0.02 ohm
I=5A ,0805

Michael 2012/02/13
add F4901 in SB

2012/06/22 SA
Change LVDS connector

20121014 aPisa SB Charles
Add comm-mode choke, EMC Cap
for PCH to LVDS

20121112 aPisa -1A Charles
Add F7-U to mount only when 70 SKU

20121206 Charles
Add EMI solution

down size/cost Charles 20121004

LVDS For Scalar

LVDS For PCH

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN / CVR

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 39 of 73

SSID = VIDEO *HDMI Level Shifter & CONNECTOR*

20120709 Jerry
Delete HDMI out Function

«Core Design»
Wistron Corporation
HDMI OUT
aPISA
SA

HDMI-IN

Use 62.10078.041 30u -> NG for production
-1A change to use 62.10078.291 and check
alternate source

HDMI

41,56 HDMI1_D2+
41,56 HDMI1_D2-
41,56 HDMI1_D1+
41,56 HDMI1_D1-
41,56 HDMI1_D0+
41,56 HDMI1_D0-
41,56 HDMI1_CK+
41,56 HDMI1_CK-

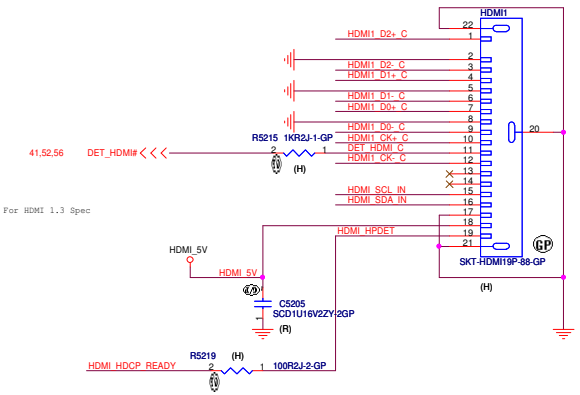
check!

41,52,56 DET_HDMI#

56 DDC_WP
41,56 HDMI1_SDA
41,56 HDMI1_SCL

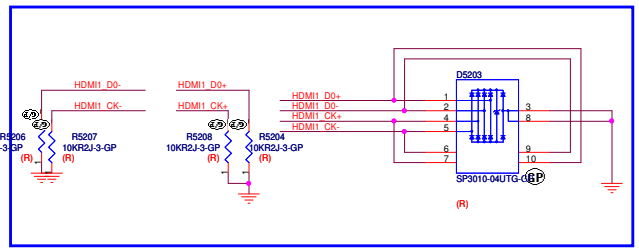
56 HDMI_HDCP_READY

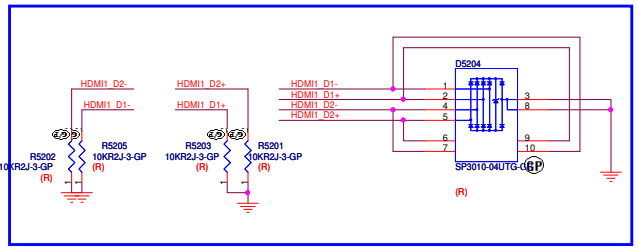
Connector



7/2 Richard
Del the resistor for NV suggestion.

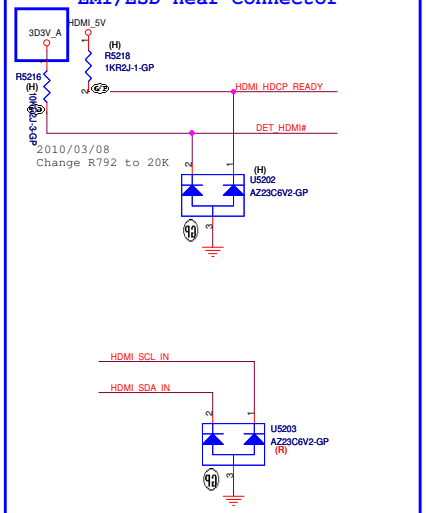
EMI/ESD near Connector

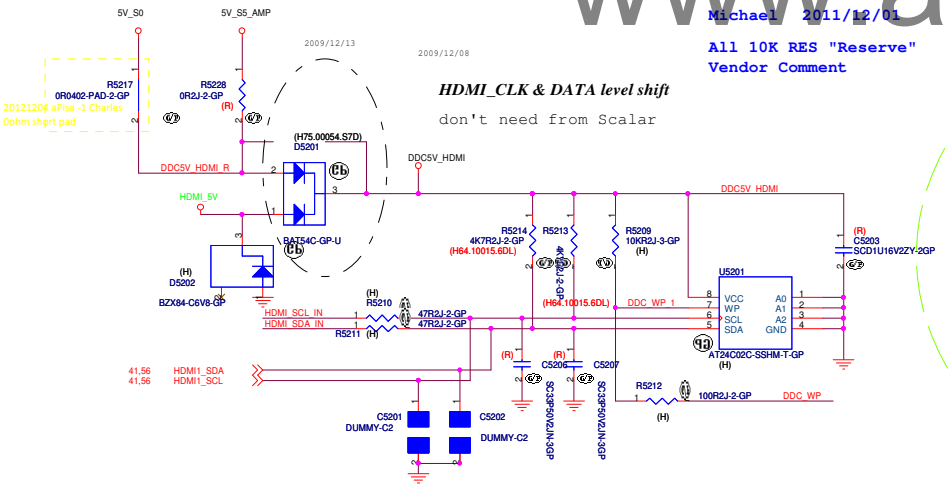




change the 3D3V_S5 to 3D3V_A

EMI/ESD near Connector





HDMI_CLK & DATA level shift

don't need from Scalar

Michael 2011/12/01

All 10K RES "Reserve"
Vendor Comment

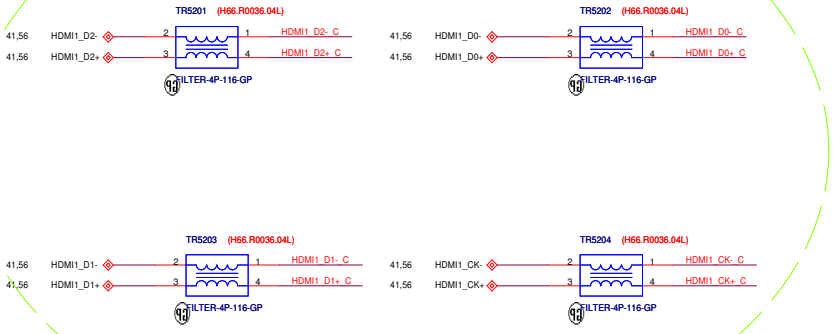
Michael 2011/12/01

change R283 and R305 from 100ohm to 47ohm

Vendor Comment

Michael 2011/12/02
Add 0ohm and unmount
Common mode chloke

Down size/cost Charles 20121004



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI IN

Size	Document Number	Rev
C	aPISA	SA

Date: Thursday, December 20, 2012 Sheet 41 of 73

2012/08/18_aPisa_SA
Delete G-SENSOR

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

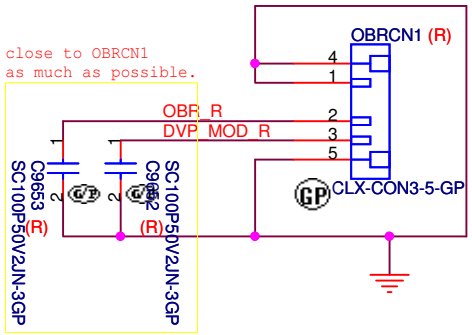
Title: G-SENSOR

Size	Document Number	Rev
Custom	aPISA	SA

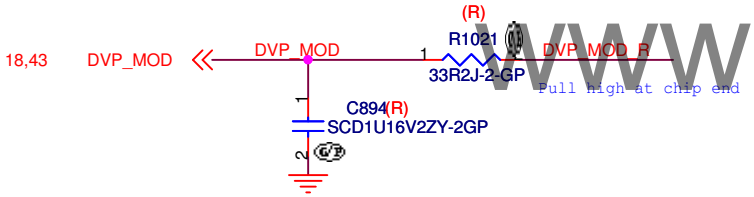
Date: Thursday, December 20, 2012 Sheet 42 of 73

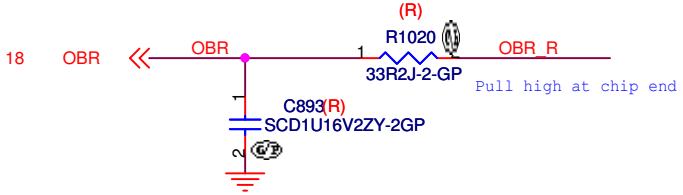
Chrome OBR Fun

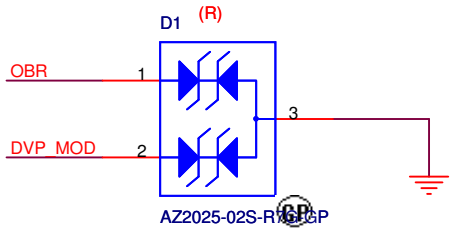
2012/09/07_aPisa_SA
Add OBR Button

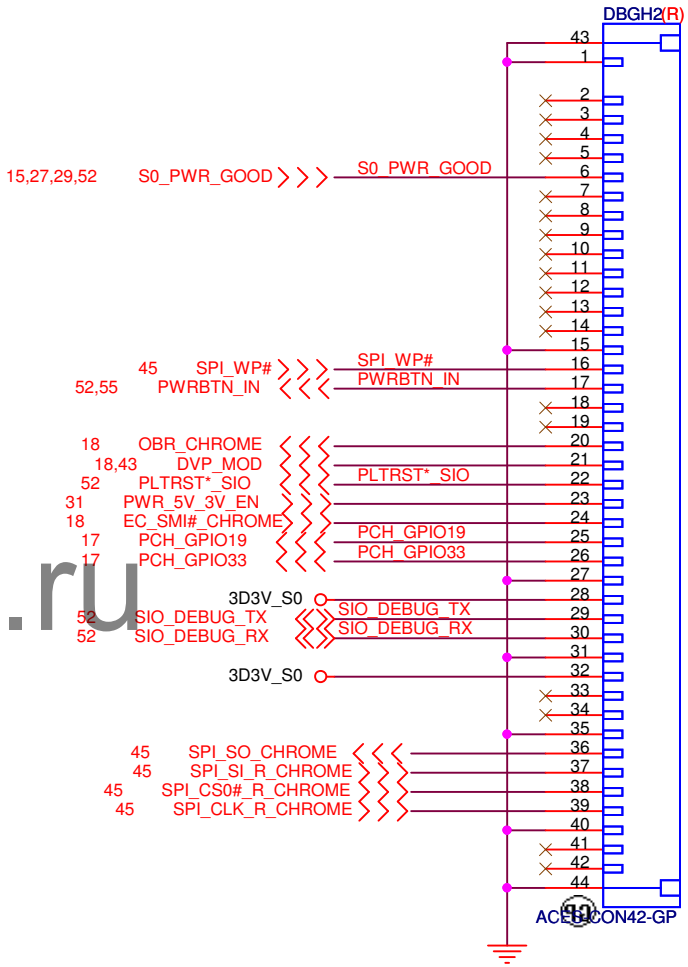


20121205 Charles
Add EMI solution









<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ChromeOS OBR / Debug connector

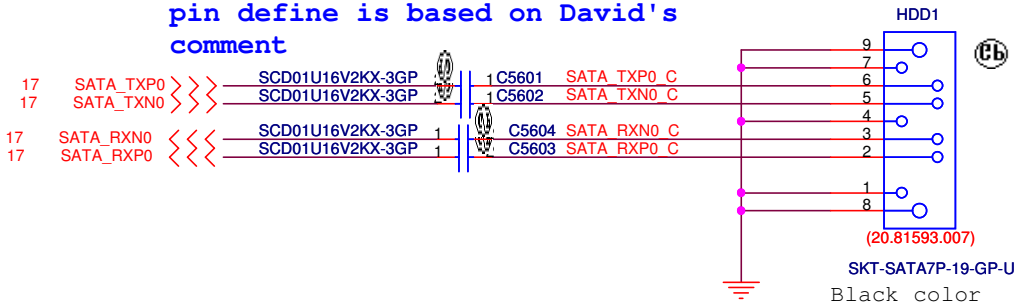
Size	Document Number	Rev
A4	aPISA	SA

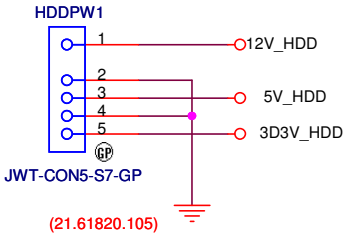
Date: Thursday, December 20, 2012 Sheet 43 of 73

SSID = SATA

SATA HDD Connector

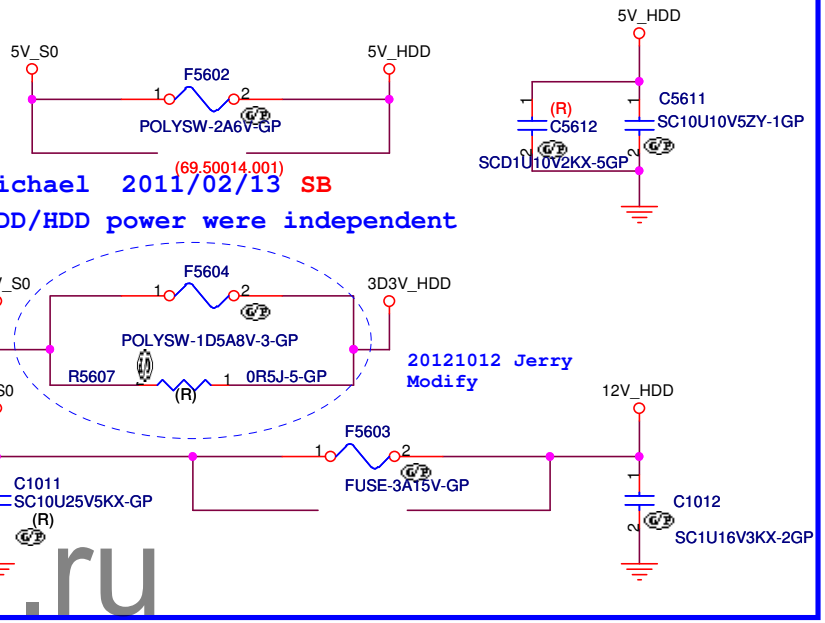
Michael 2012/01/03
pin define is based on David's comment

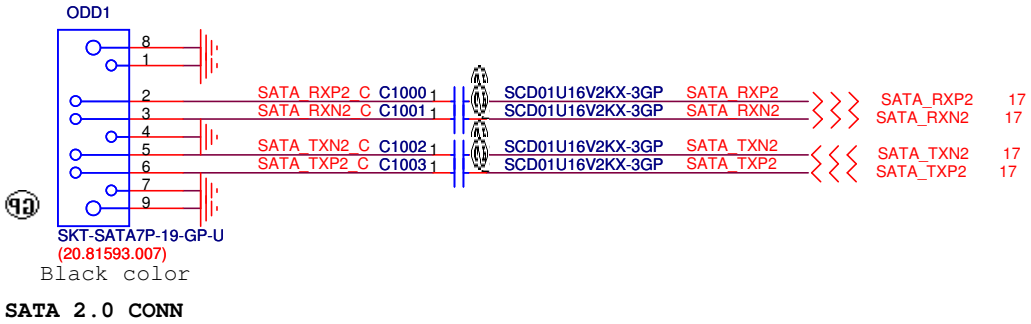




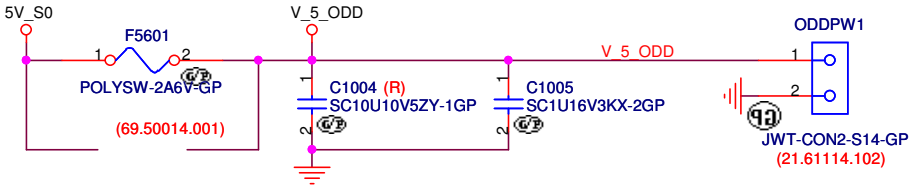
2012/08/18_aPisa_SA

Layout: Put them together

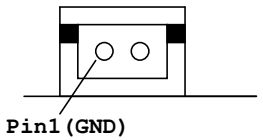




ODD SATA POWER CONNECTOR



Front View



2012/08/18_aPisa_SA
ADD ODD

20.60341.104: 4pin right angle
20.60334.103: 3pin right angle

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

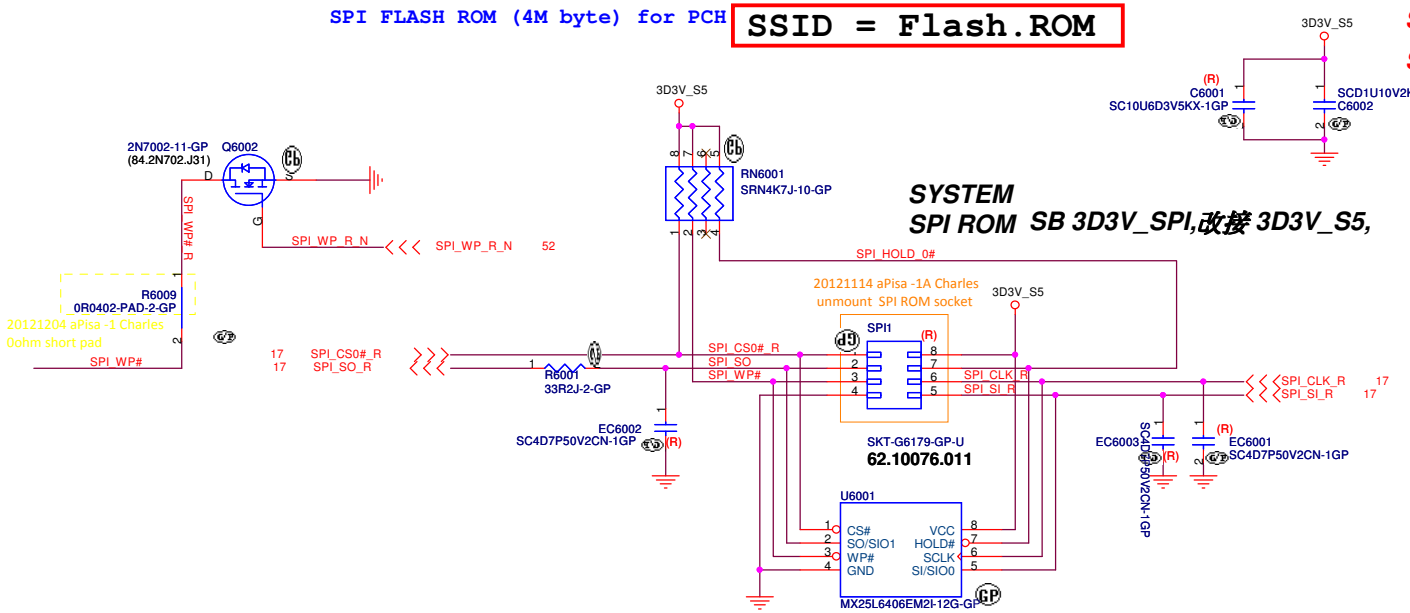
Title	HDD/ODD	
Size: Custom	Document Number: aPISA	Rev: SA
Date: Thursday, December 20, 2012	Sheet 44 of 73	

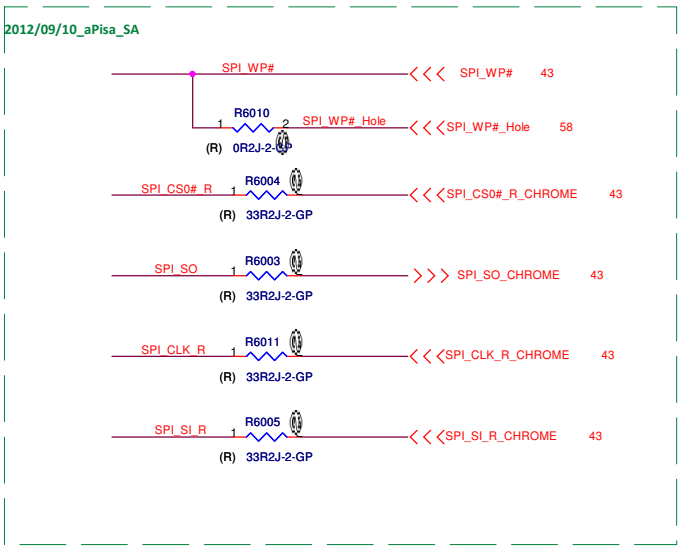
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

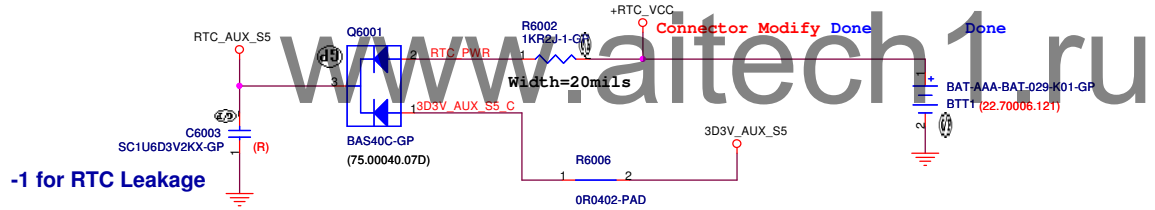
SPI ROM Equal length need to less than 500mil





2012/01/03

SSID = RBATT

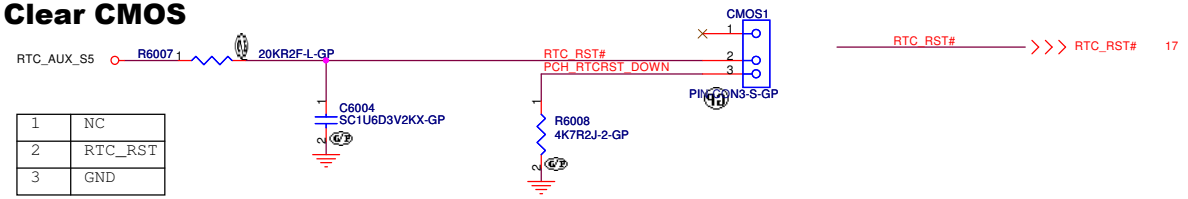


-1 for RTC Leakage

2011/9/30

Add CLR CMOS circuit

Clear CMOS



1	NC
2	RTC_RST
3	GND

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

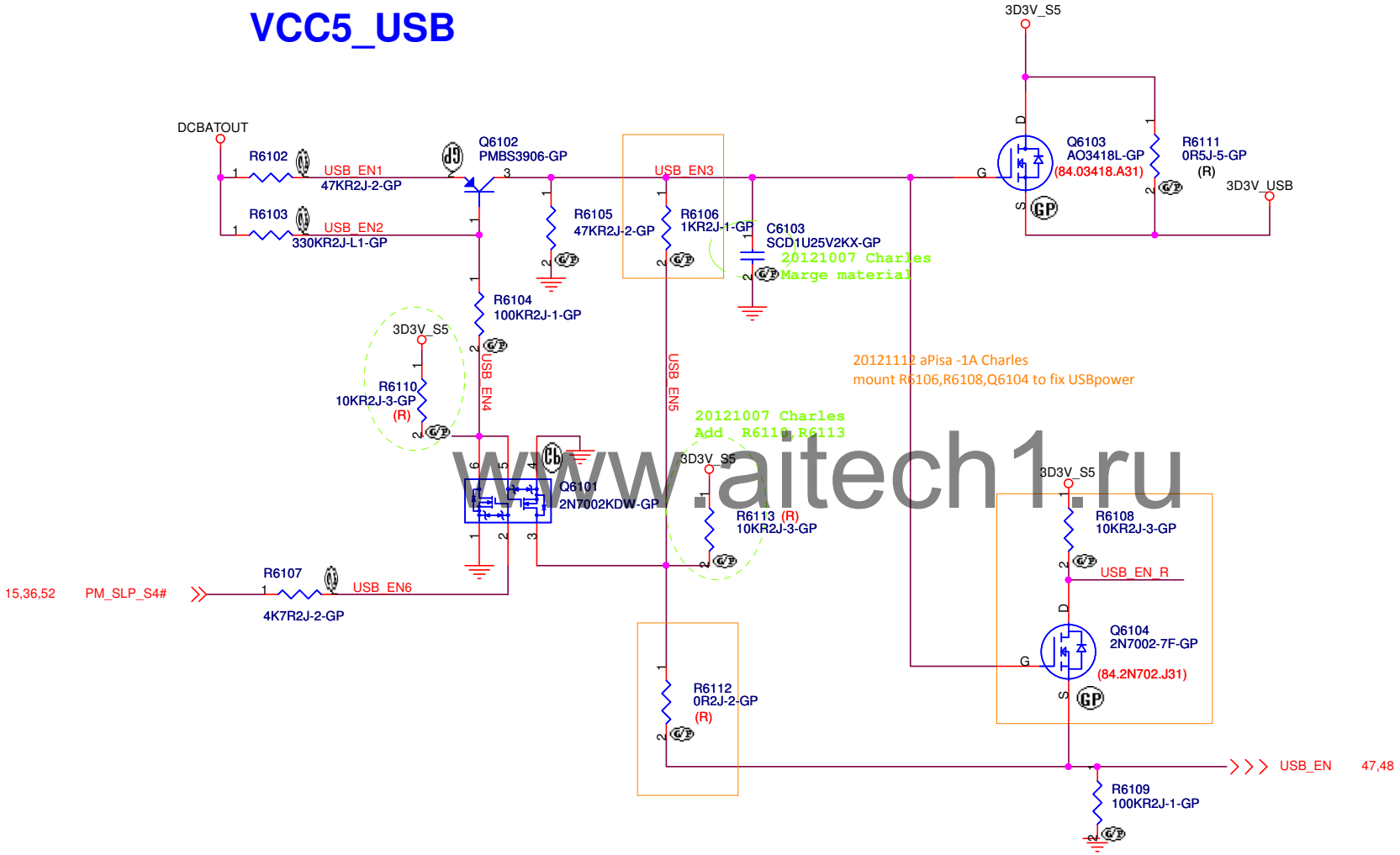
Title: SPI/RTC

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 45 of 73

SSID = USB

VCC5_USB



<Core Design>

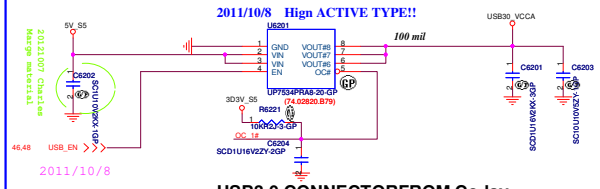
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB2.0 Power SW**

Size	Document Number	Rev
Custom	aPISA	SA

Date: Thursday, December 20, 2012 Sheet 46 of 73

2011/10/8 Hign ACTIVE TYPE!!

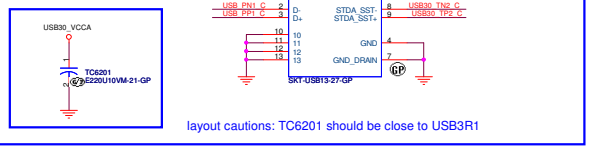


2011/10/8

USB3.0 CONNECTORFROM Co-lay

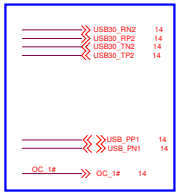
2012/07/09 Jerry
Delete USB3.0 Port

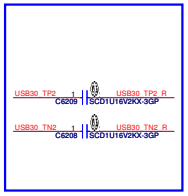
2012/08/18_aPisa_SA
Change USB3.0 symbol



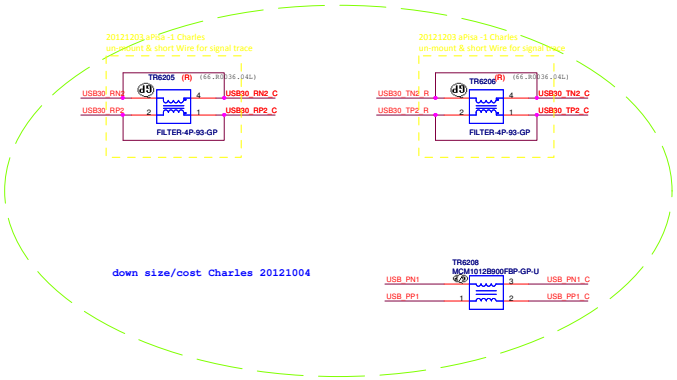
layout cautions: TC6201 should be close to USB3R1

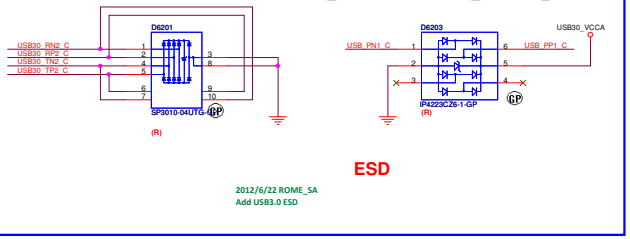
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	





2011/10/12
EMI





ESD

2012/6/22 ROME_SA
Add USB3.0 ESD

2012/08/18_aPisa_SA
Delete Charger

<Core Design>

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Title: USB 3.0 Port

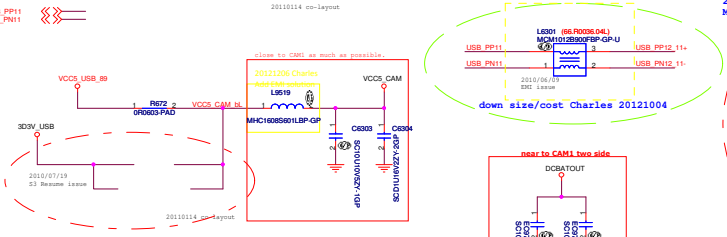
Size	Document Number	Rev
Custom	aPISA	SA

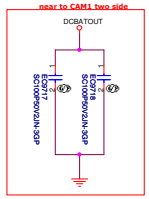
Date: Thursday, December 20, 2012 Sheet 47 of 73

SSID =USB2.0

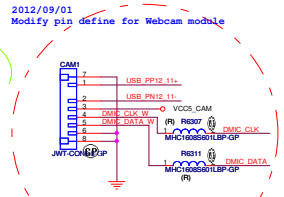
USB Port12 -> WEB CAM

2011/10/18



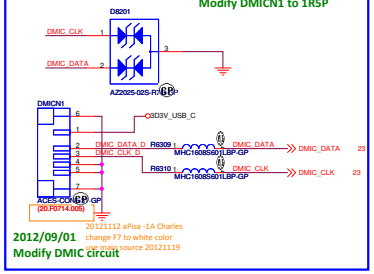


2012/09/01
Modify pin define for Webcam module



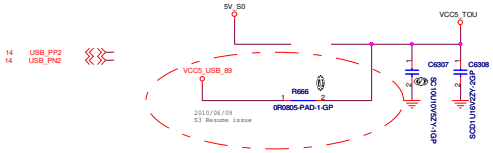
DMIC Connector

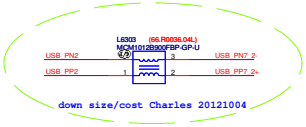
2012/09/07
Modify DMICN1 to 1R5P

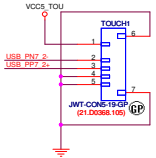


2012/06/29 Jerry
Delete RF Function

USB Port 7 -> TOUCH



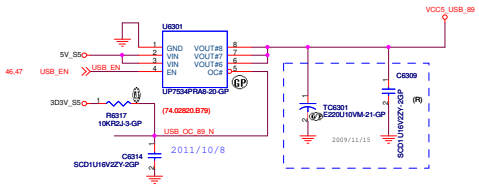


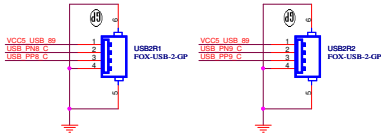


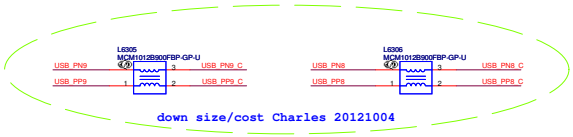
2012/06/29 Jerry
Delete IR Function

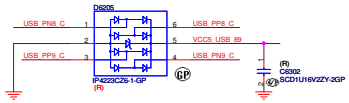
USB Port 8,9-> REAR I/O

Reserve EMI
CMN Choke









<Core Design>
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Title: Rear USB/TOU/Dongle/Web Cam
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 48 of 73

SSID = Wireless and Bluetooth

2011/11/29
Michael
ADD USB for BT Function

Mini Card Connector(Wireless LAN+BT)

2012/06/26_ROME SA Change symbol to 5.2mm

Michael 2011/11/29
Change 1D5V_MEM to 1D5V_S0

Height: 5.2mm
T-CONN: 62.10043.831
BELLWETHER: 62.10043.A81

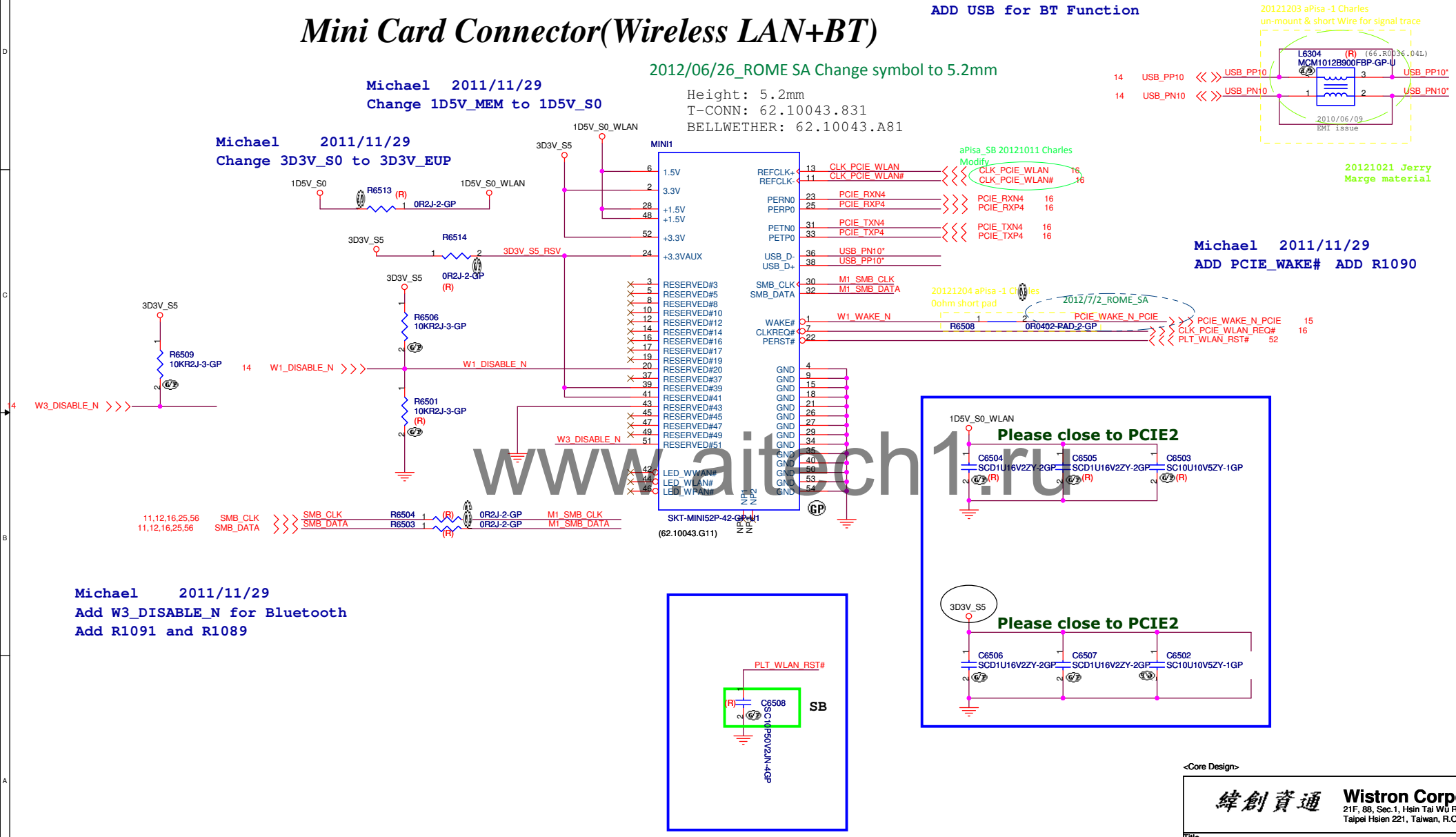
Michael 2011/11/29
Change 3D3V_S0 to 3D3V_EUP

20121203 aPisa -1 Charles
un-mount & short Wire for signal trace

20121021 Jerry
Marge material

Michael 2011/11/29
ADD PCIE_WAKE# ADD R1090

Michael 2011/11/29
Add W3_DISABLE_N for Bluetooth
Add R1091 and R1089



<Core Design>

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Title: Mini PCIE Card WLAN / BT

Size	Document Number	Rev
Custom	aPISA	SA

Date: Thursday, December 20, 2012 Sheet 49 of 73

2012/08/18_aPisa_SA

Delete mSATA

<Core Design>

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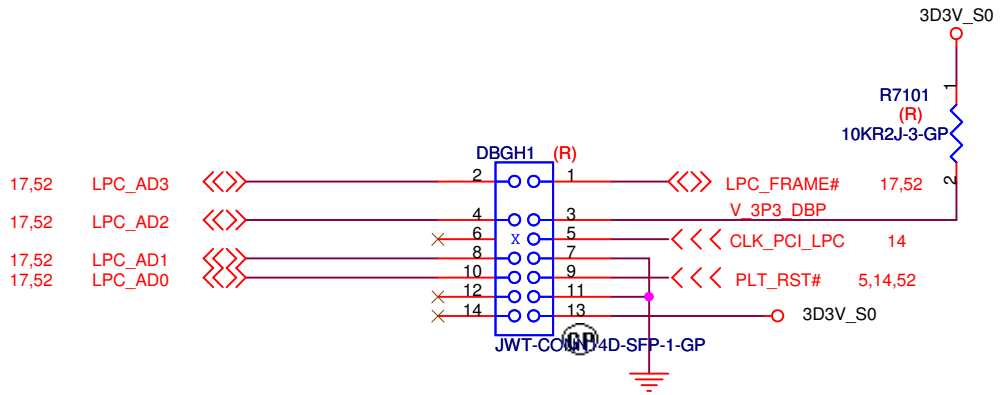
Title: Mini PCIE Card mSATA

Size	Document Number	Rev
Custom	aPISA	SA

Date: Thursday, December 20, 2012 Sheet 50 of 73

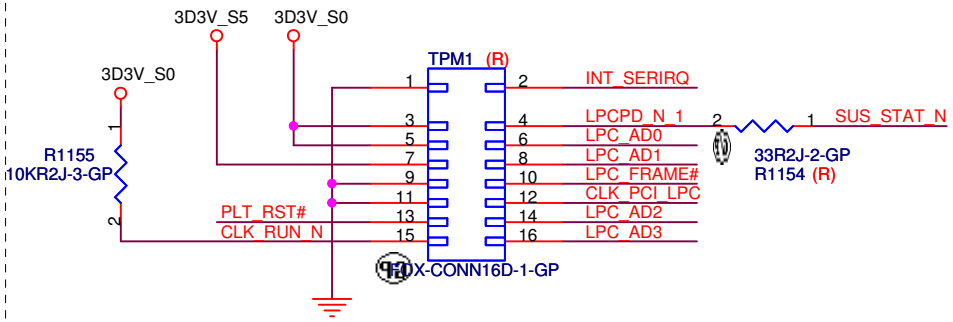


17,52 INT_SERIRQ

15 SUS_STAT_N

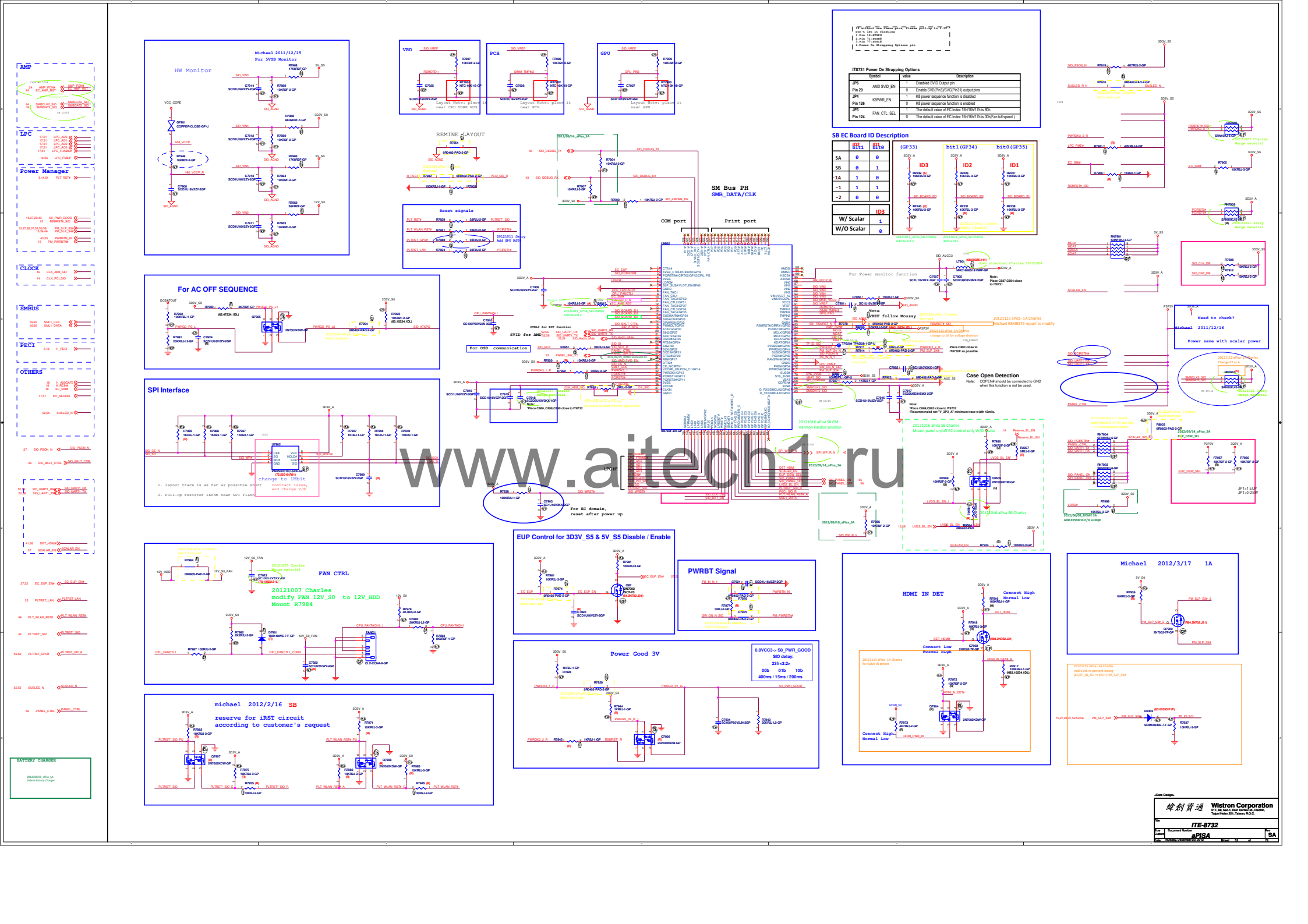
TPM Header

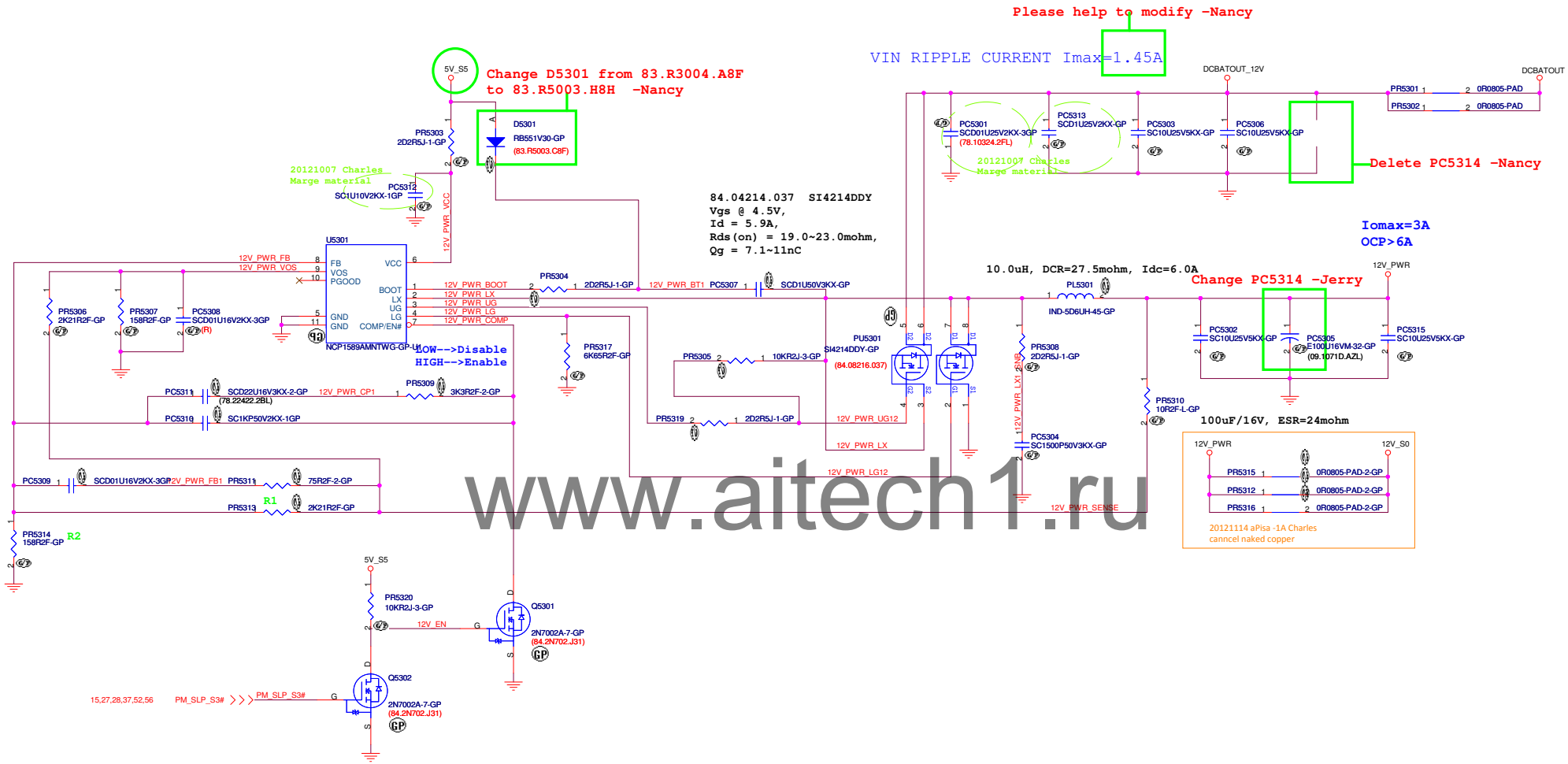
2012/09/07_aPisa_SA
Add TPM Header



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Debug connector***		
Size: A4	Document Number: ***aPISA***	Rev: SA
Date: Thursday, December 20, 2012	Sheet 51 of 73	





<Core Design>

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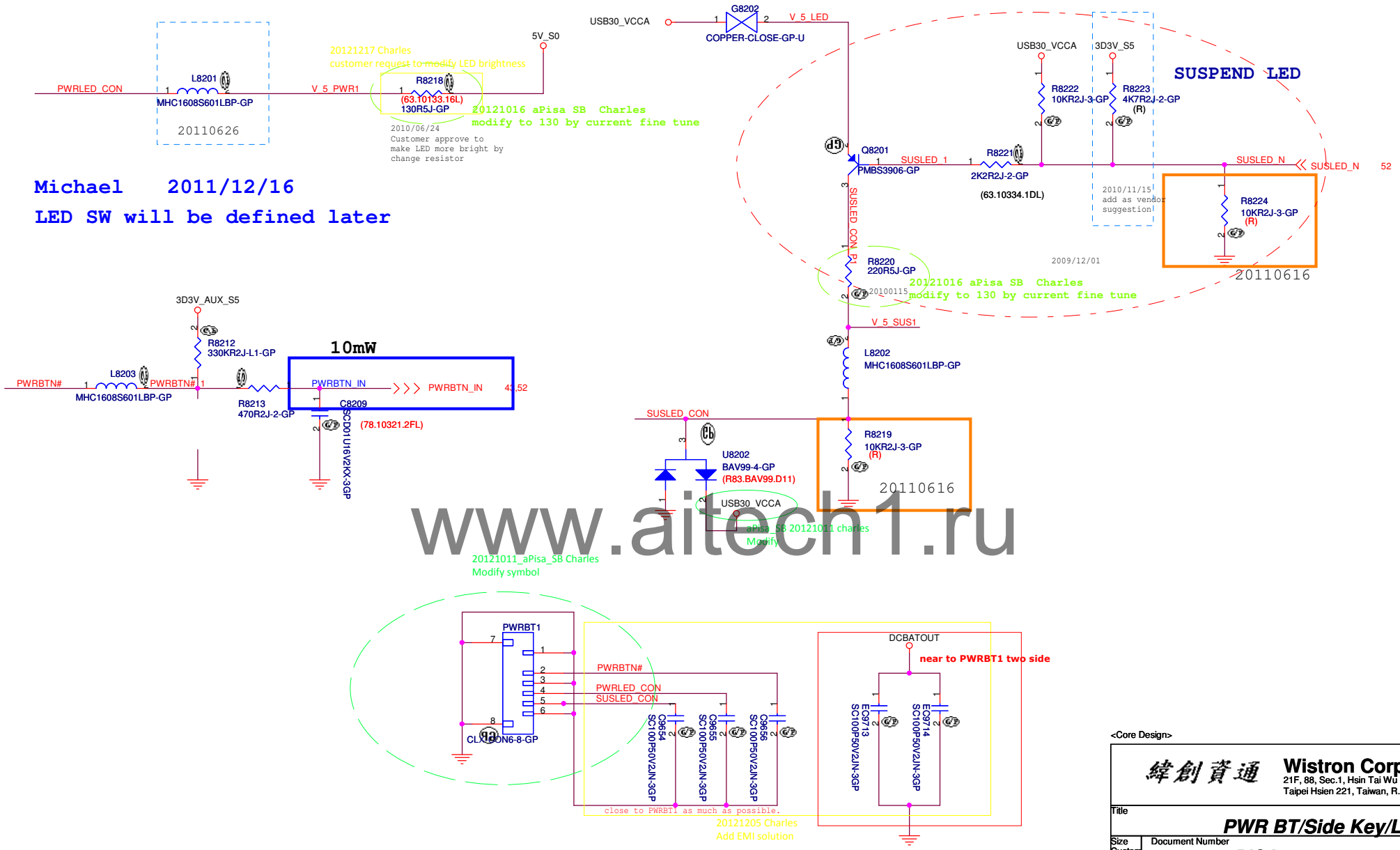
Title: 12V

Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 53 of 73

2012/08/18_aPisa_SA
Delete Battery Charger



<Core Design>

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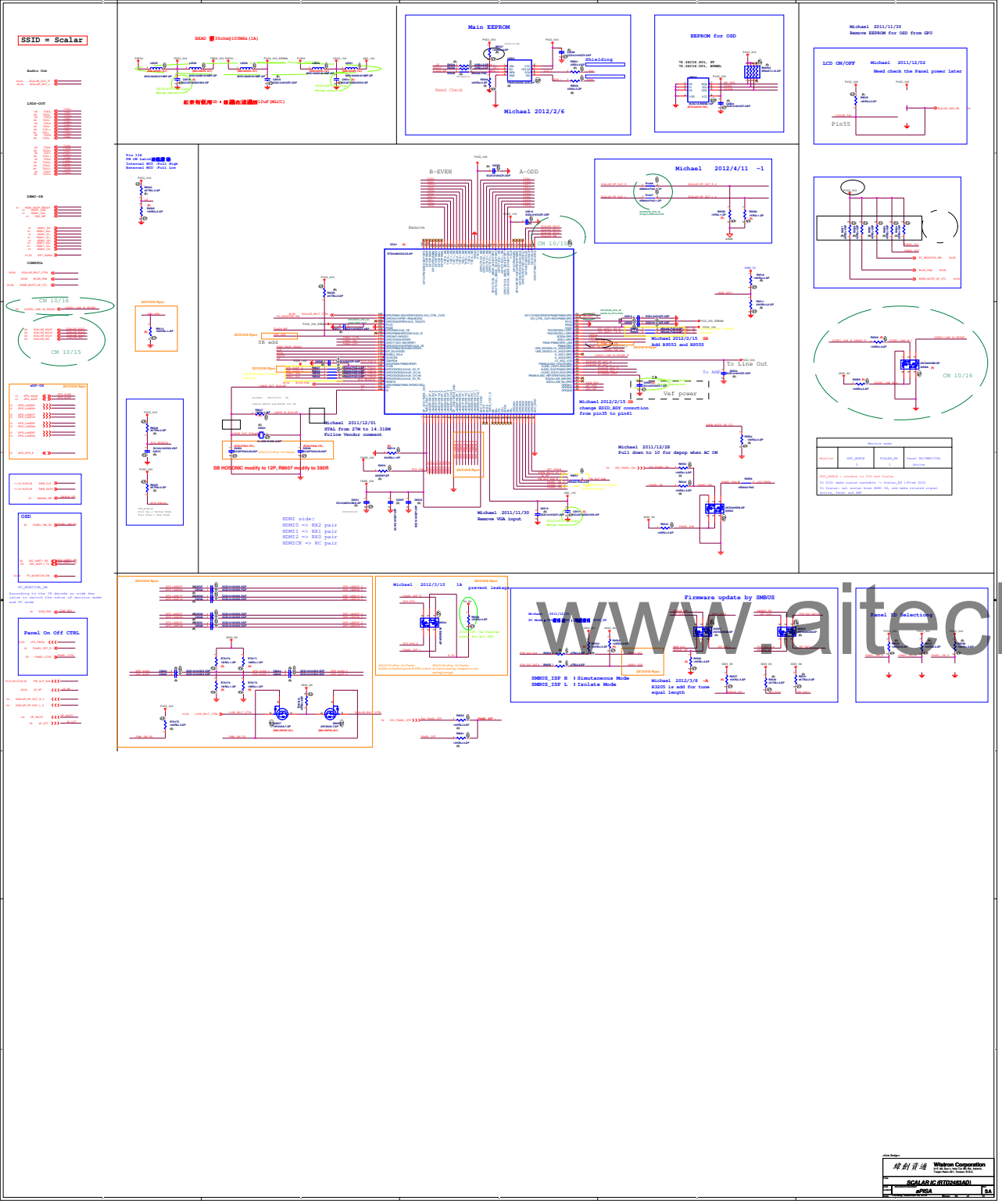
Title: PWR BT/Side Key/LED

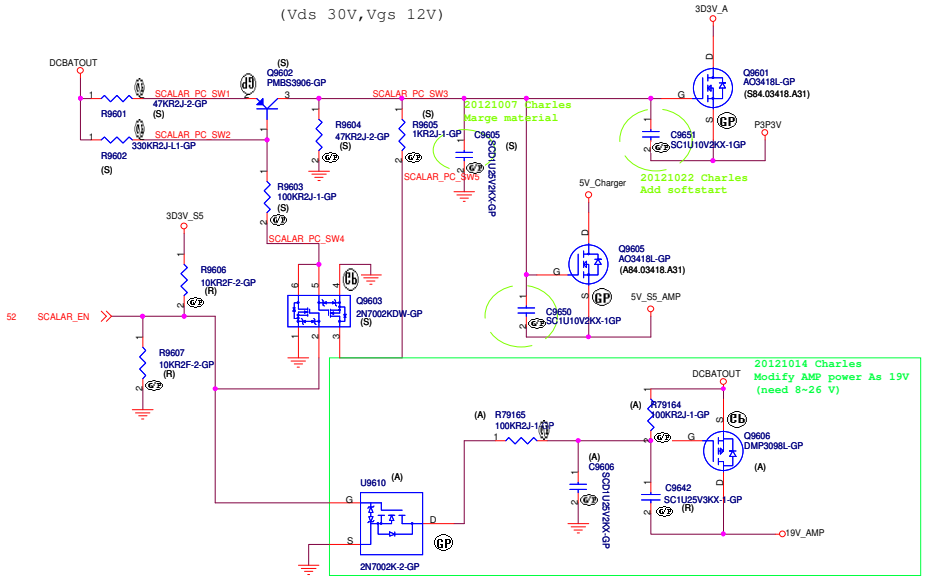
Size: Custom | Document Number: aPISA | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 55 of 73

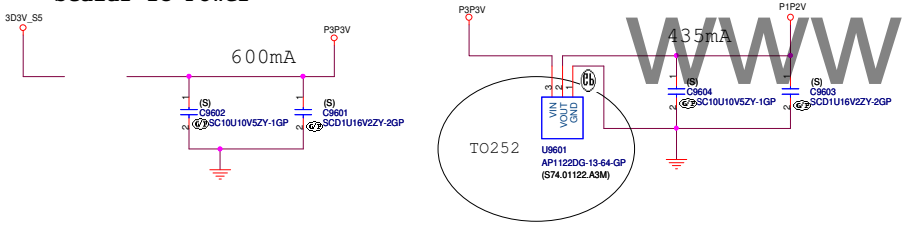


SSID = SDIO

AO3418 NMOS 3.1A, 60mohm,Vgs=10V **Michael 2011/12/01**
NMOS H: Enable L:Disable **change 5V_S5 to 5V_Charger**
3.1A 60 mohm(10V)
(Vds 30V,Vgs 12V)



Scalar IC Power



Scalar Spec Table

	GPI input	From	High	Low	Default
Pin69	GPI-1 PC Power ON → PM_SLP_S3# 15,27,28,37,52,53,56	SB	PC	Monitor	Monitor
Pin109	GPI-2 Mode change/ Panel OnOff	SW	Normal	Touch	PC: PC (PC->HDMI) Monitor: HDMI, VGA (HDMI)

	GPO output				
Pin55	GPO-2 Panel On/OFF → SCALAR_VDD_EN 39,56	Scalar	ON	OFF	PC: ON Monitor: Detect Signal
Pin104	GPO-3 PC/Monitor → PC_MONITOR_SW 24,56	Scalar	PC	Monitor	PC: PC, Monitor: HDMI, VGA
Pin101	GPO-5 Video → BLON_EN# 39,56	Scalar	Disable	Enable	Disable
Pin72	GPO-6 Audio Mute → SHDN_MUTE_AP_CTL 24,56	Scalar	on-Mute	MUTE	MUTE

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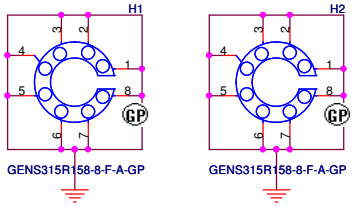
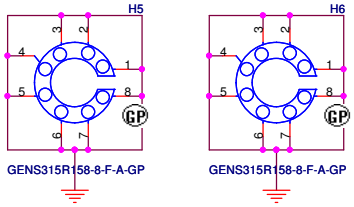
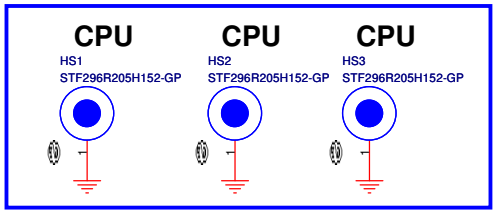
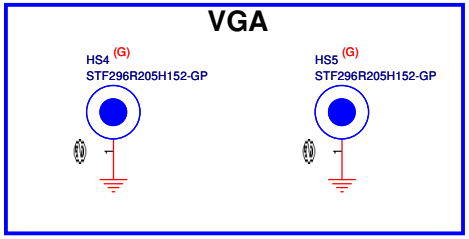
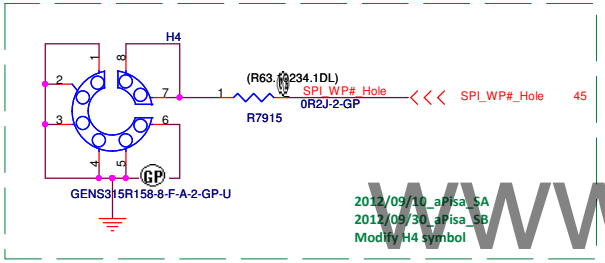
Title: SCALAR POWER (RTD2483AD)
Size: Custom | Document Number: aPISA | Rev: SA
Date: Thursday, December 20, 2012 | Sheet 57 of 73

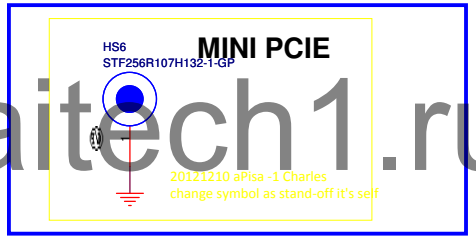


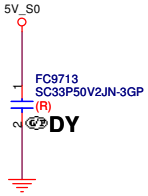


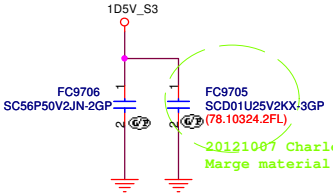


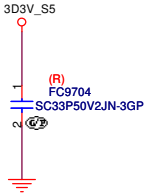


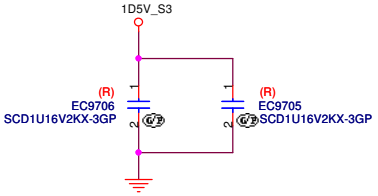












<Core Design>

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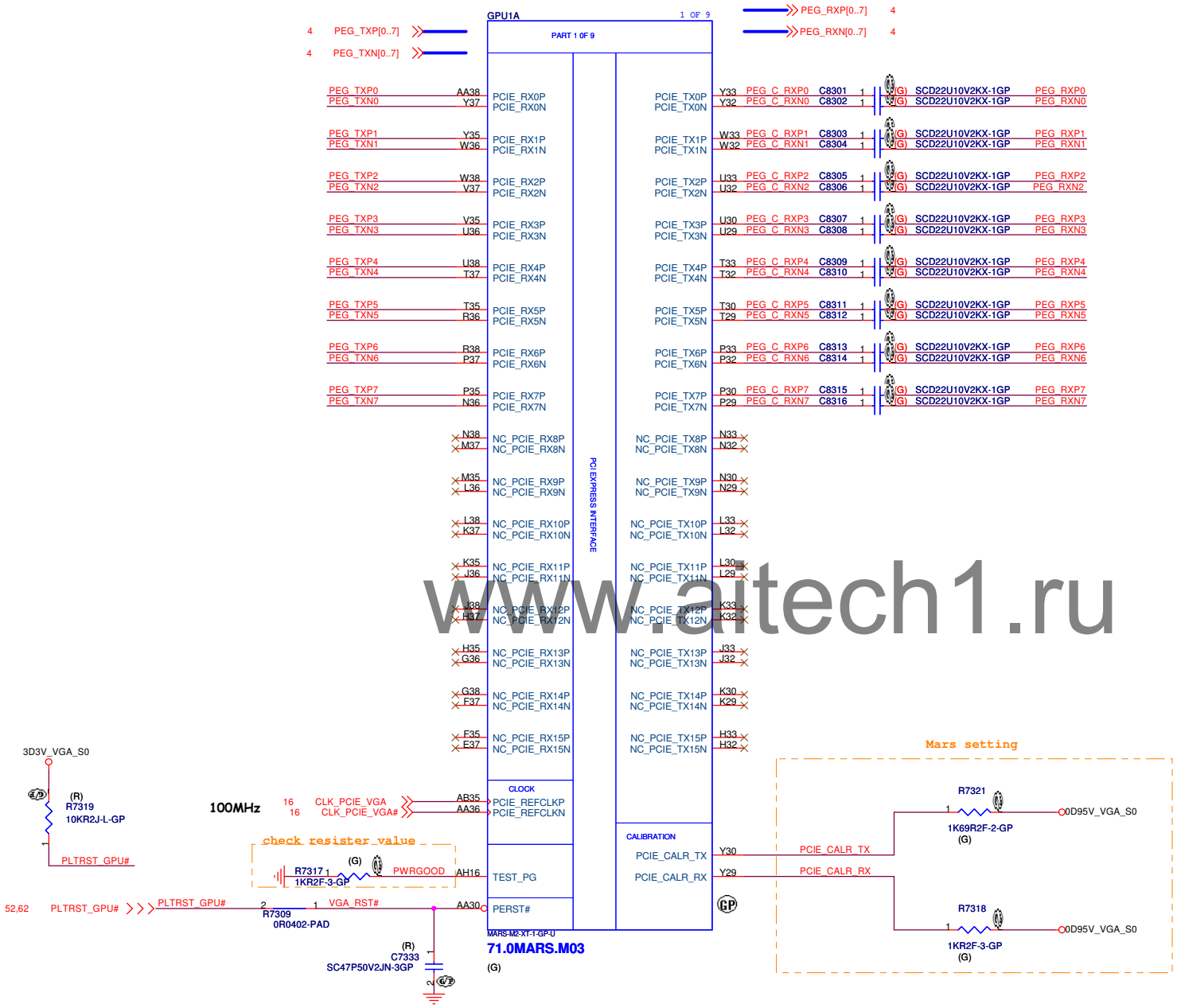
Title: STAND OFF/HOLE/EMI CAP

Size	Document Number	Rev
A3	aPISA	SA

Date: Thursday, December 20, 2012 Sheet 58 of 73



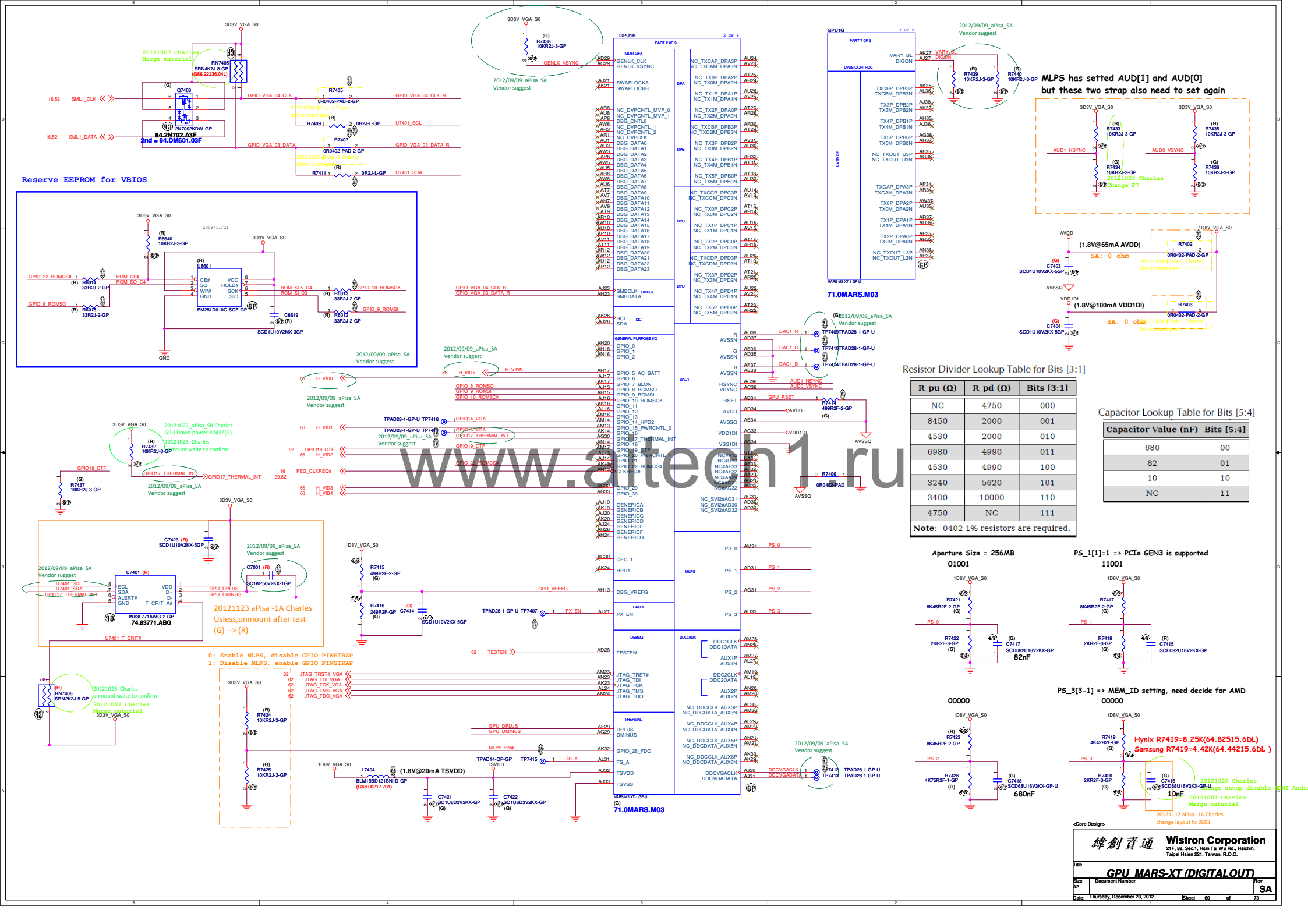
<Core Design>

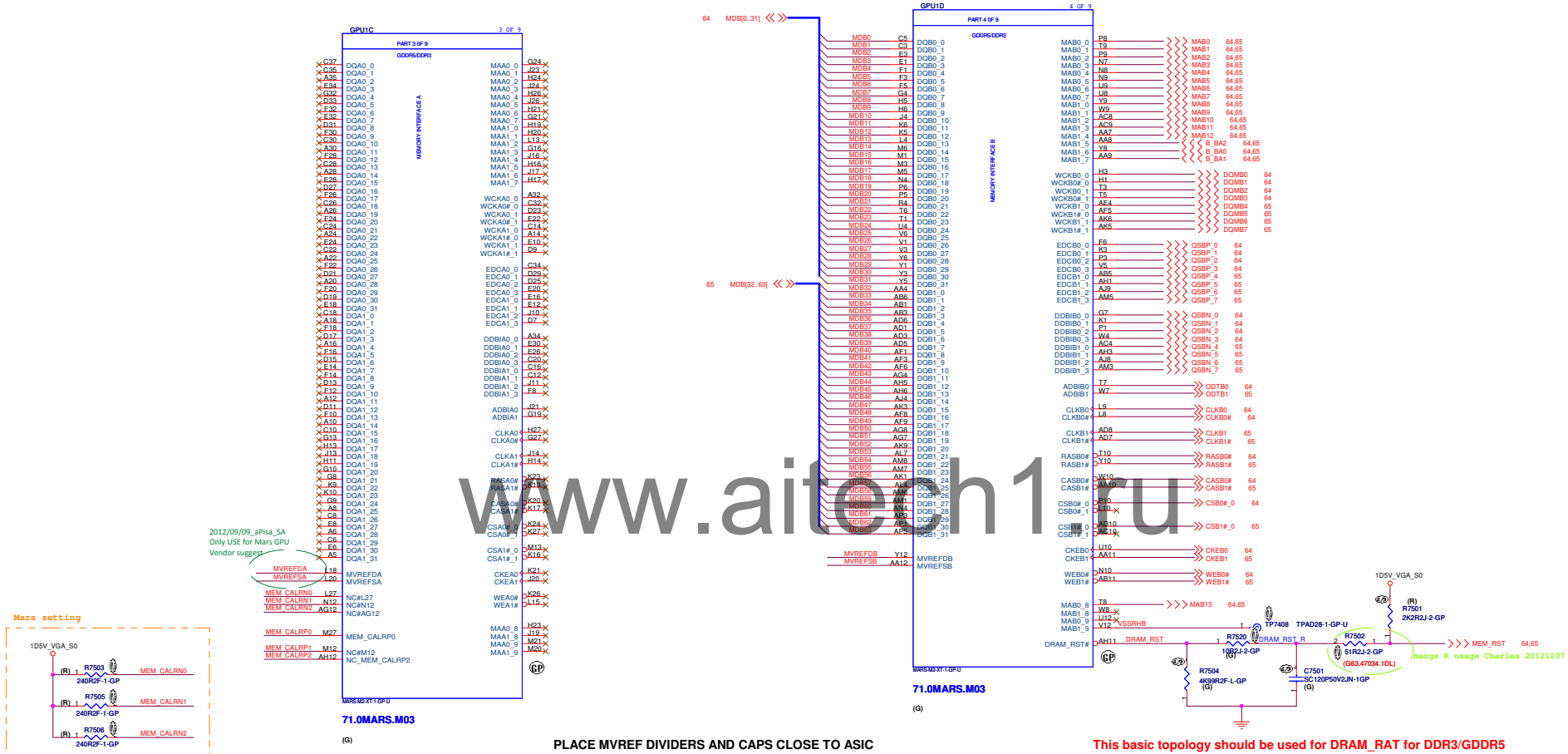
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_MARS-XT(PEG)

Size: A3 | Document Number | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 59 of 73





PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

This basic topology should be used for DRAM_RAT for DDR3/GDDR5

DDR3/GDDR3 Memory Stuff Option(Mars)

	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R
C			1uF

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F)

Size: A2 | Document Number | Rev: SA

Date: Thursday, December 20, 2012 | Sheet 61 of 73

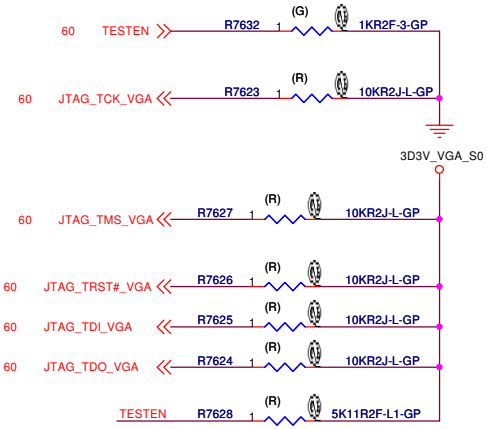
Table 3–31 Multi-level Pin Straps

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 48).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_ PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	Design dependent, see the description.
PS_1[1]	STRAP_BIF_ GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	N/A
PS_2[2]	N/A	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	Reserved	N/A
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4] PS_3[5]	AUD_PORT_CONN_ PINSTRAP[1] AUD_PORT_CONN_ PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC silicon itself, the number and type of connectors on the board (DP/ HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. This pin strap is encoded as an active low binary as follows to ensure zero enables all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.

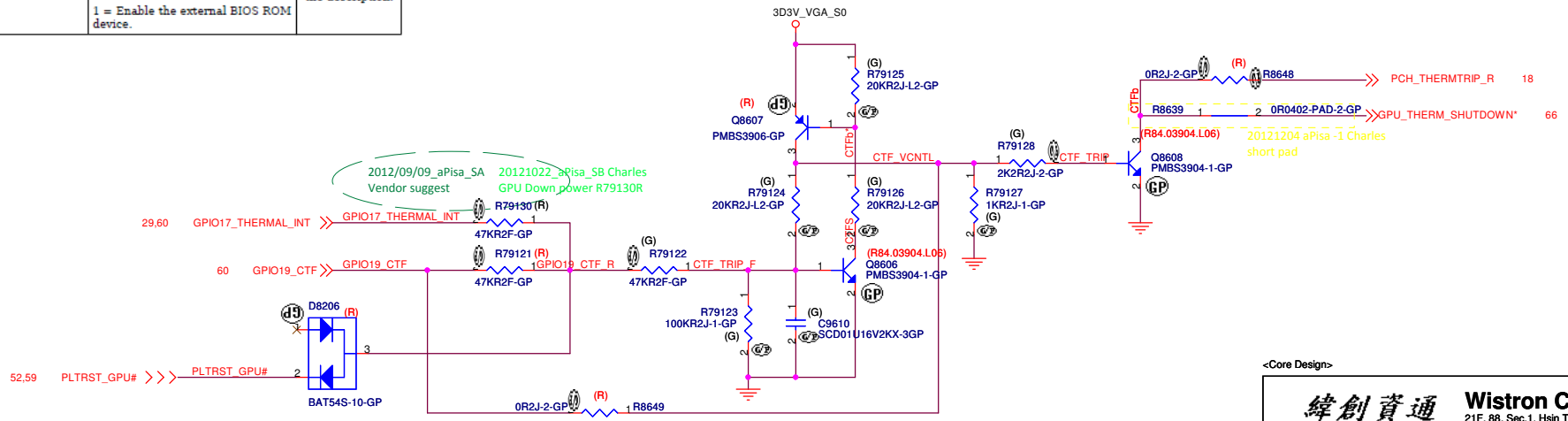
Note: AUD[1] (on HYSNC) and AUD[0] (on VSYNC) still need to be properly pin strapped even in a MLPS-based design.

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"0" (PD)	"1" (PU)	"0" (PD)
JTAG_TRST#	"1" (PU)	"1" (PU)	NC
JTAG_TCK	"0" (PD)	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC



THERMAL PROTECTION



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Title: GPU (GPIO/STRAP)

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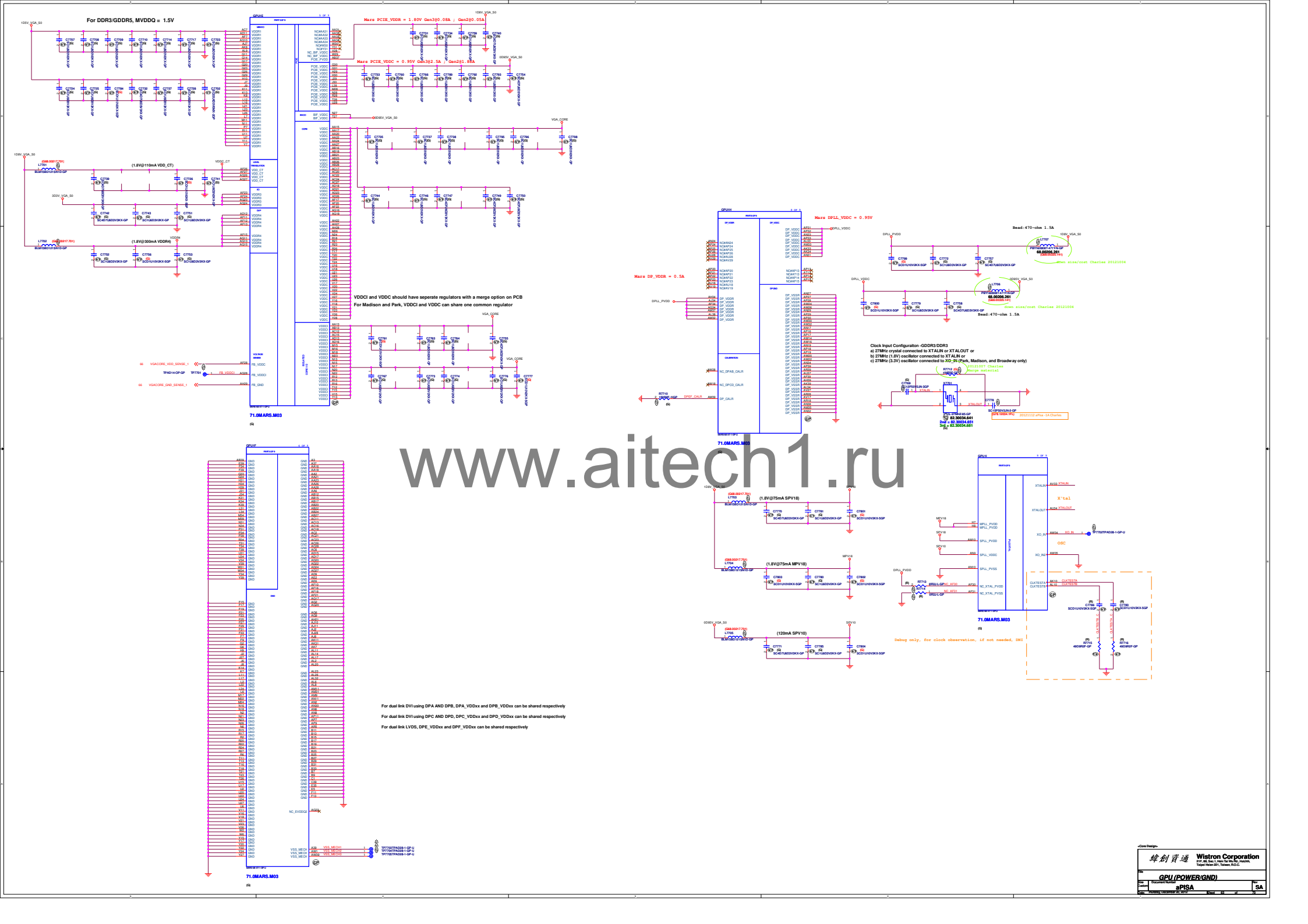

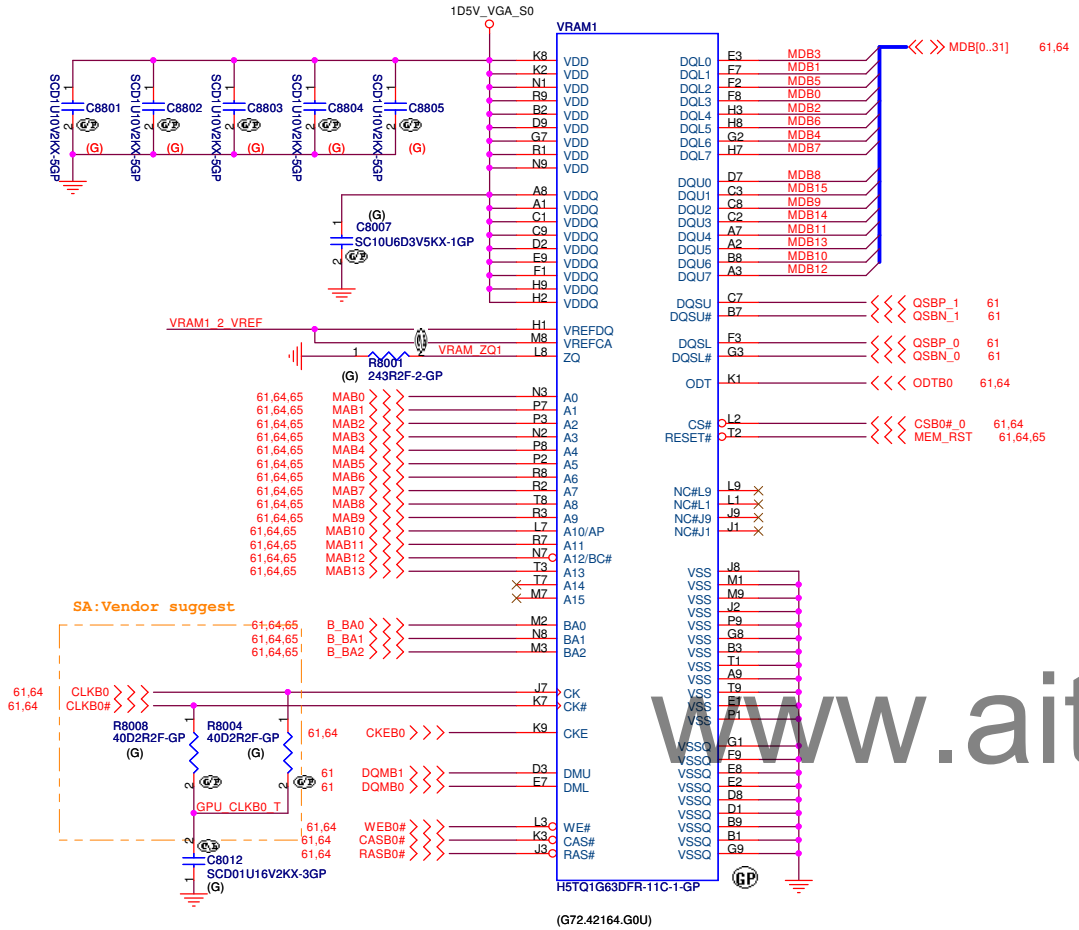

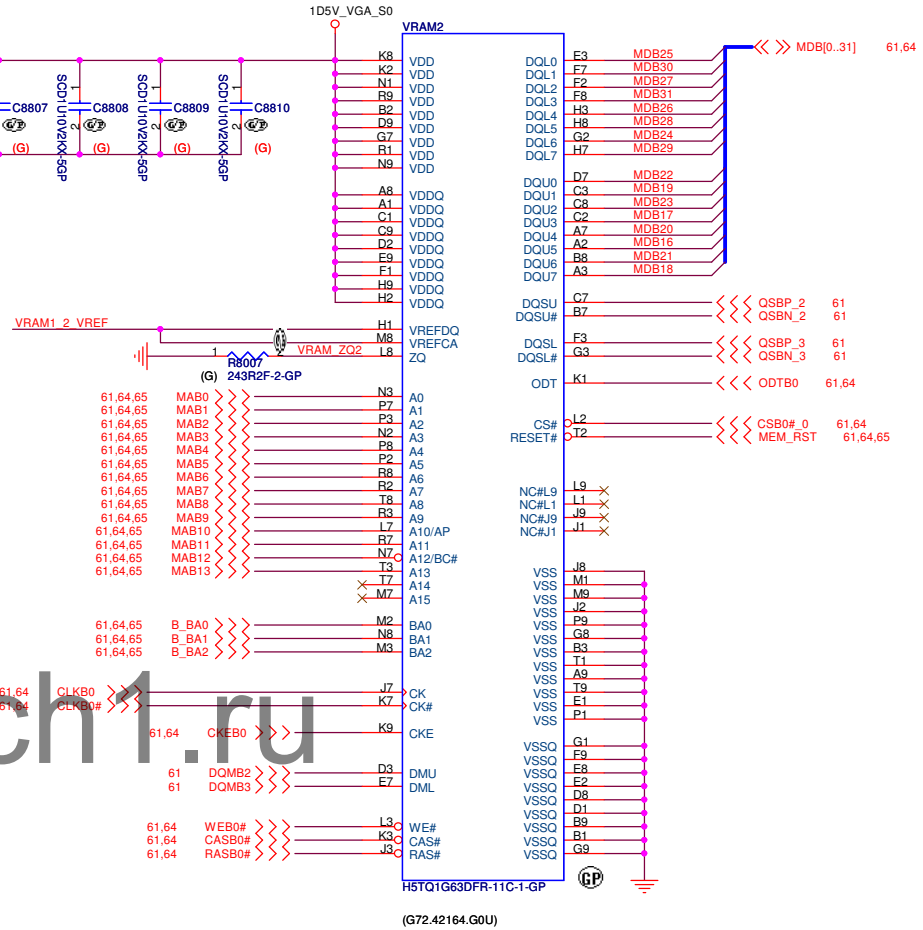

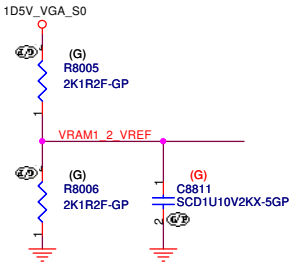

128M*16 VRAM
72.42164.G0U - SAMSUNG K4W2G1646E-BC11
72.52G63.C0U - Hynix H5TQ2G63DFR-11C

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Title: GPU-VRAM1,2

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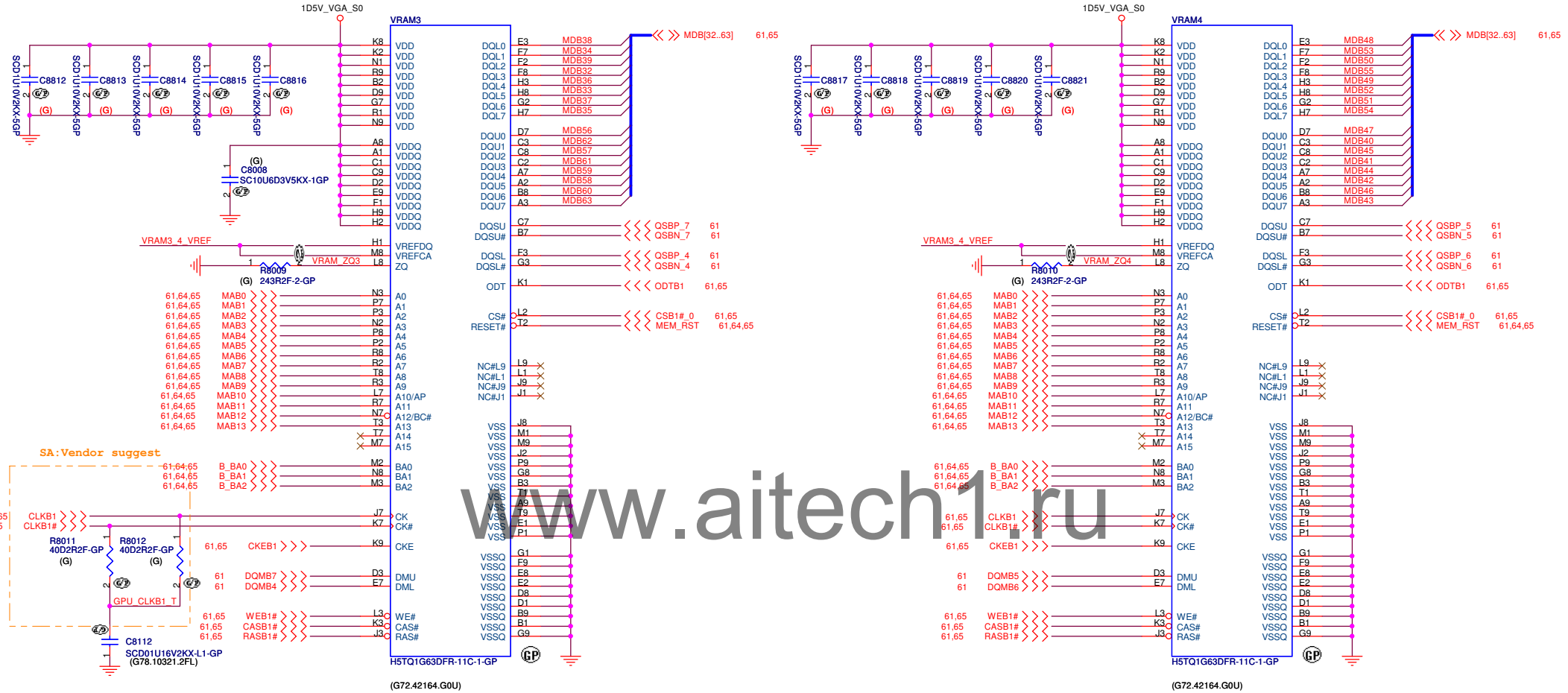

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72.52G63.C0U - Hynix H5TQ2G63DFR-11C

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Title	GPU-VRAM3,4	
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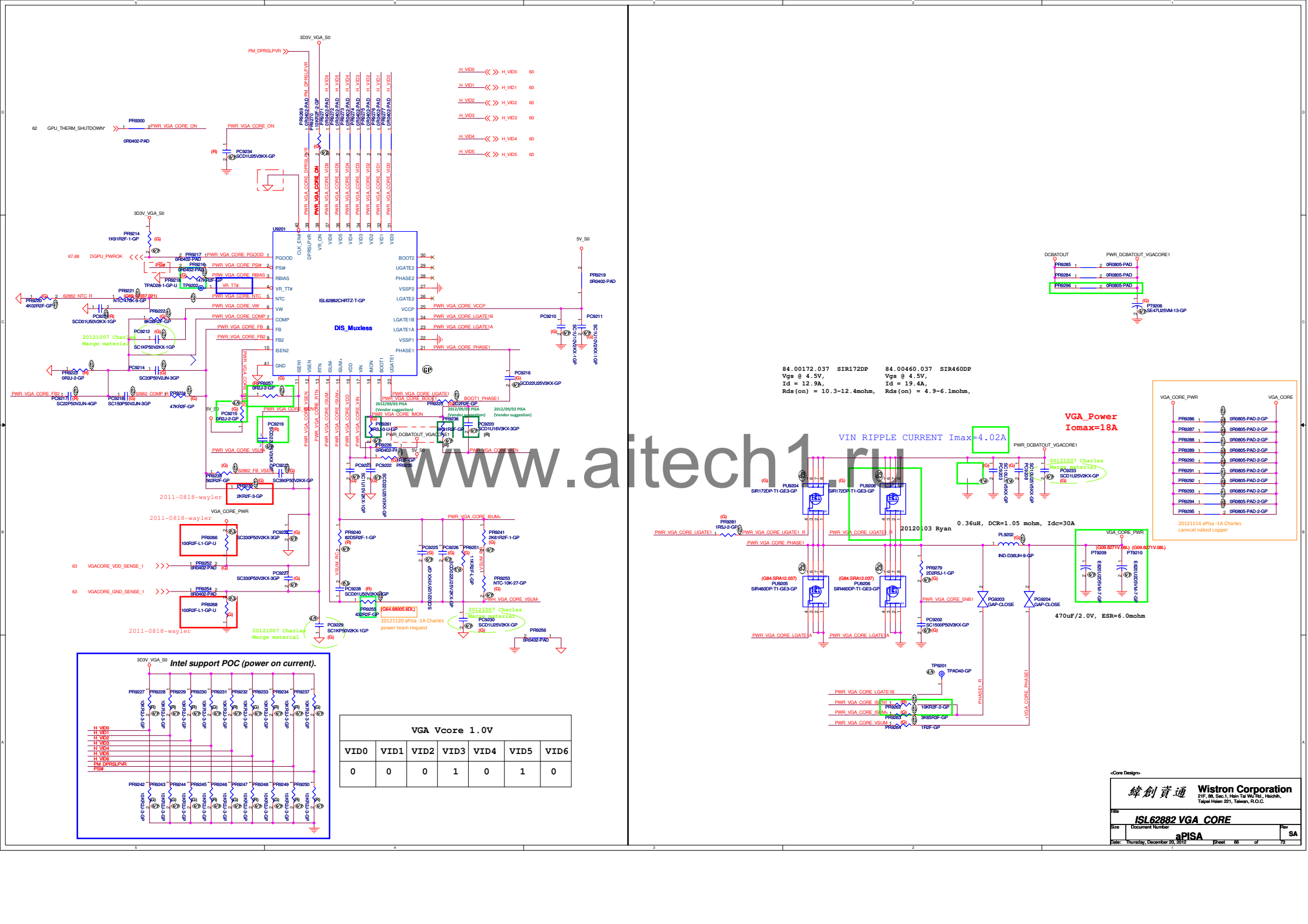

APL5912 for 0D95V_VGA_S0

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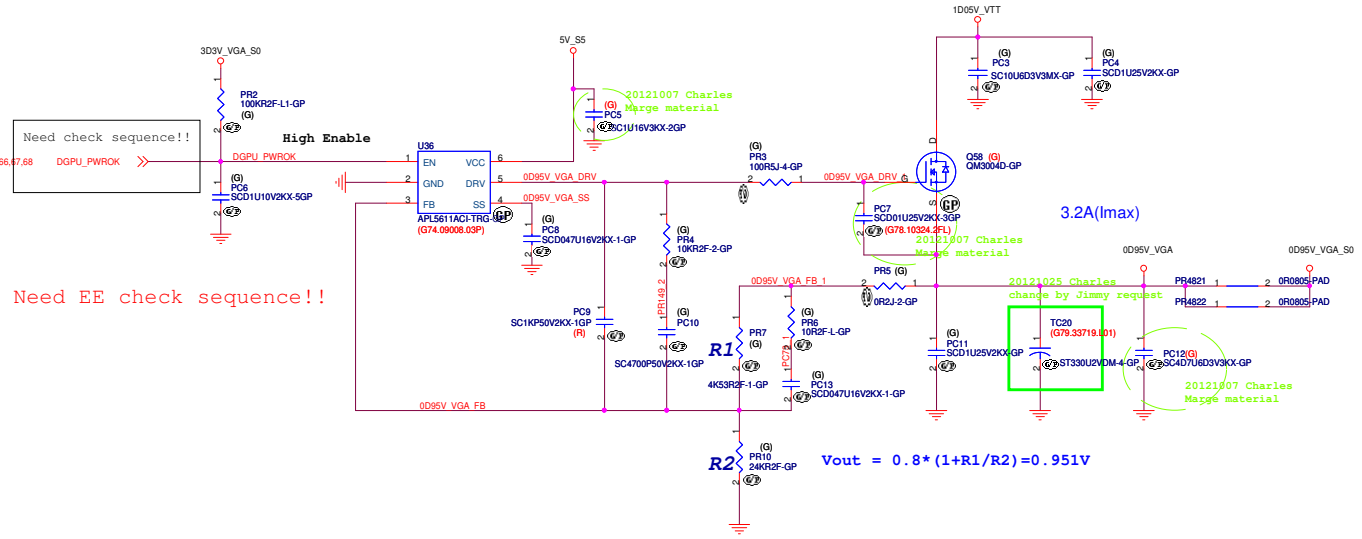

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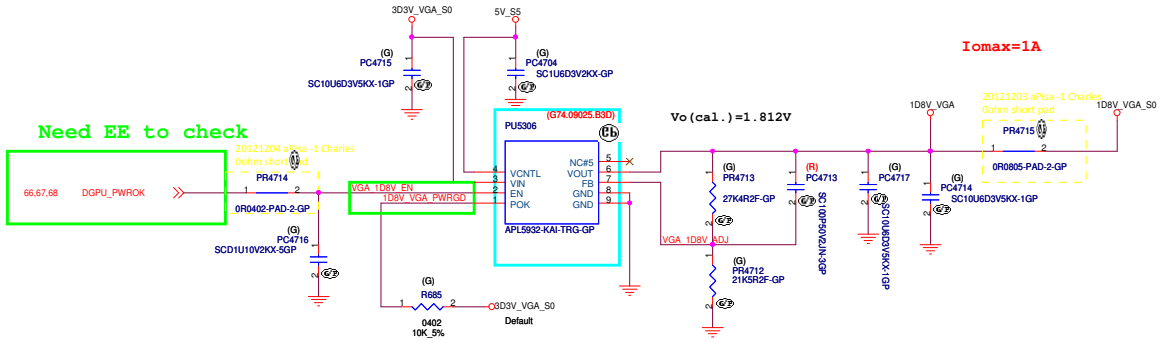

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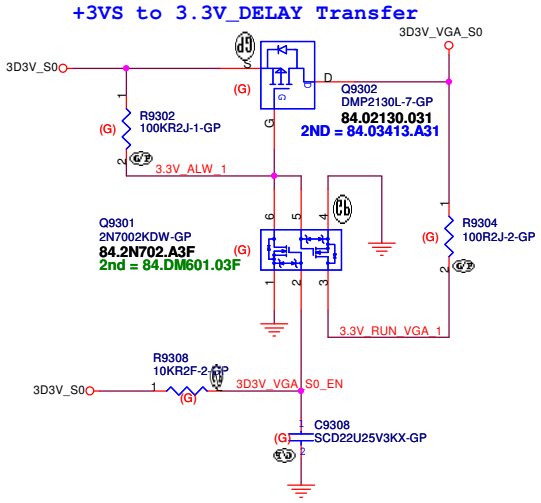
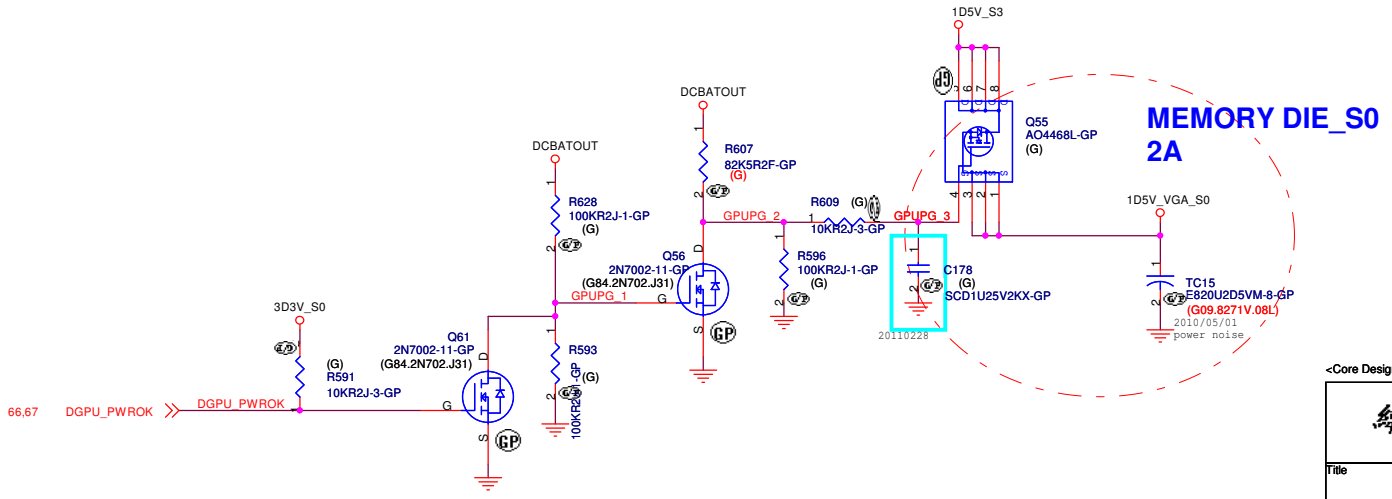
3D3V_VGA_S0



1D5V_VGA_S0

20110103
GPU VCORE -> MEMORY POWER



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Title: DISCRETE VGA POWER

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Title: NFC / Proximity

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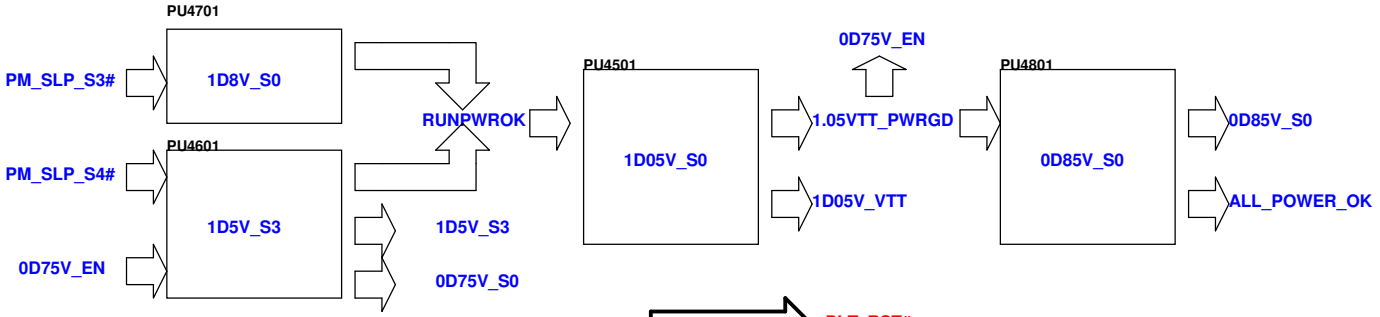
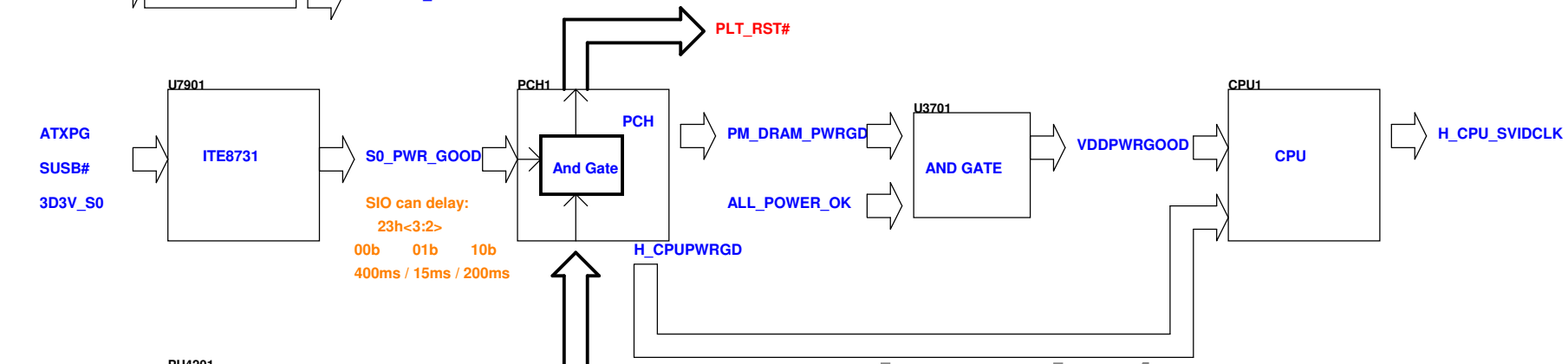
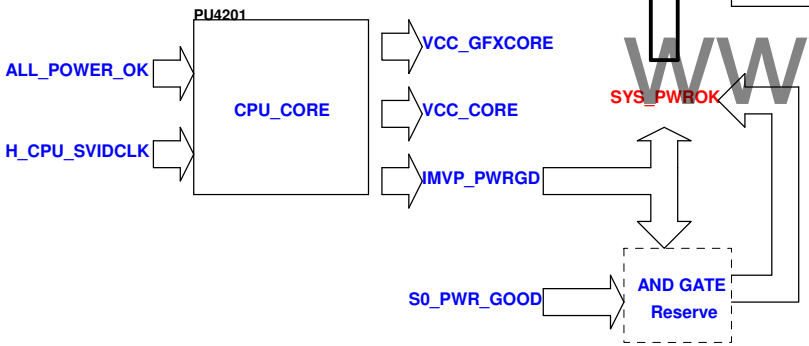
Power Sequence



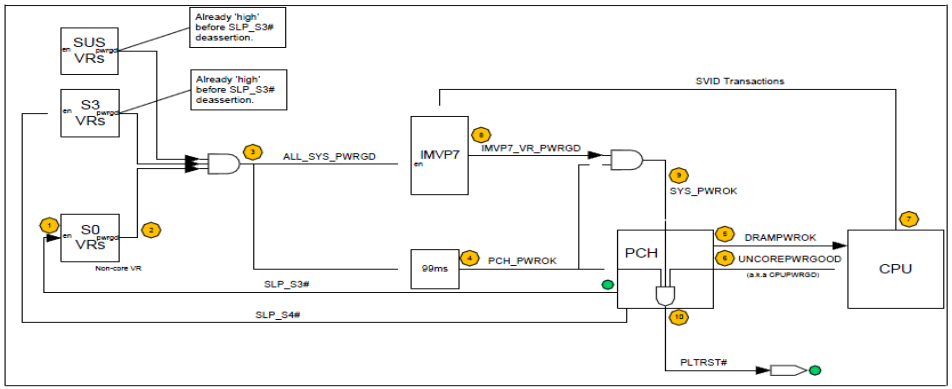




SYS_PWROK Generation

SYS_PWROK is expected to be asserted when indicating that the system is ready to release PLTRST#. Figure 2-2 shows the recommended power-on sequencing flow steps from SLP_S3# deassertion until PLTRST# is deassertion.

-2. Flow Diagram for SYS_PWROK Generation



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Title: SEQUENCE DIAGRAM		
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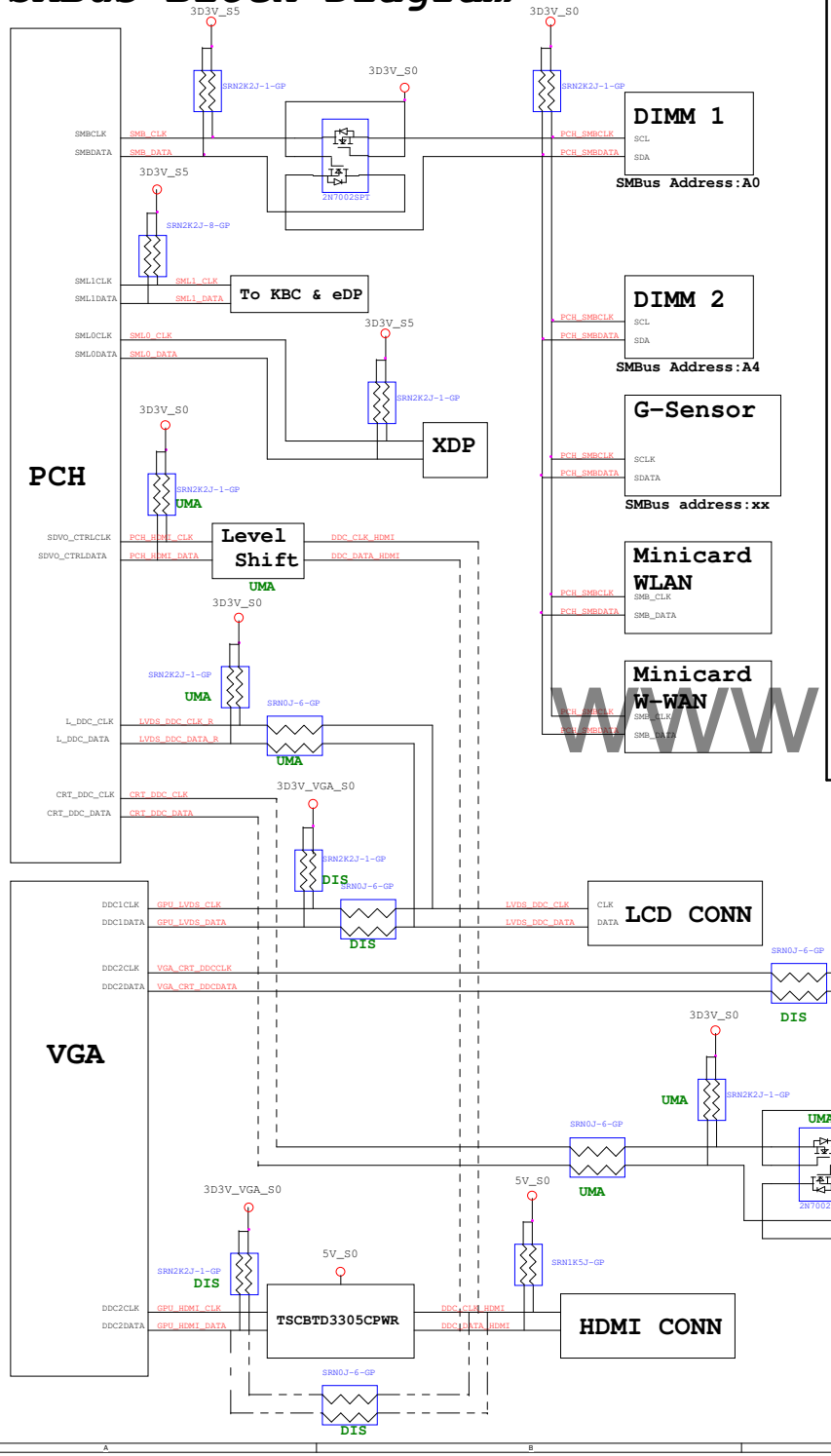
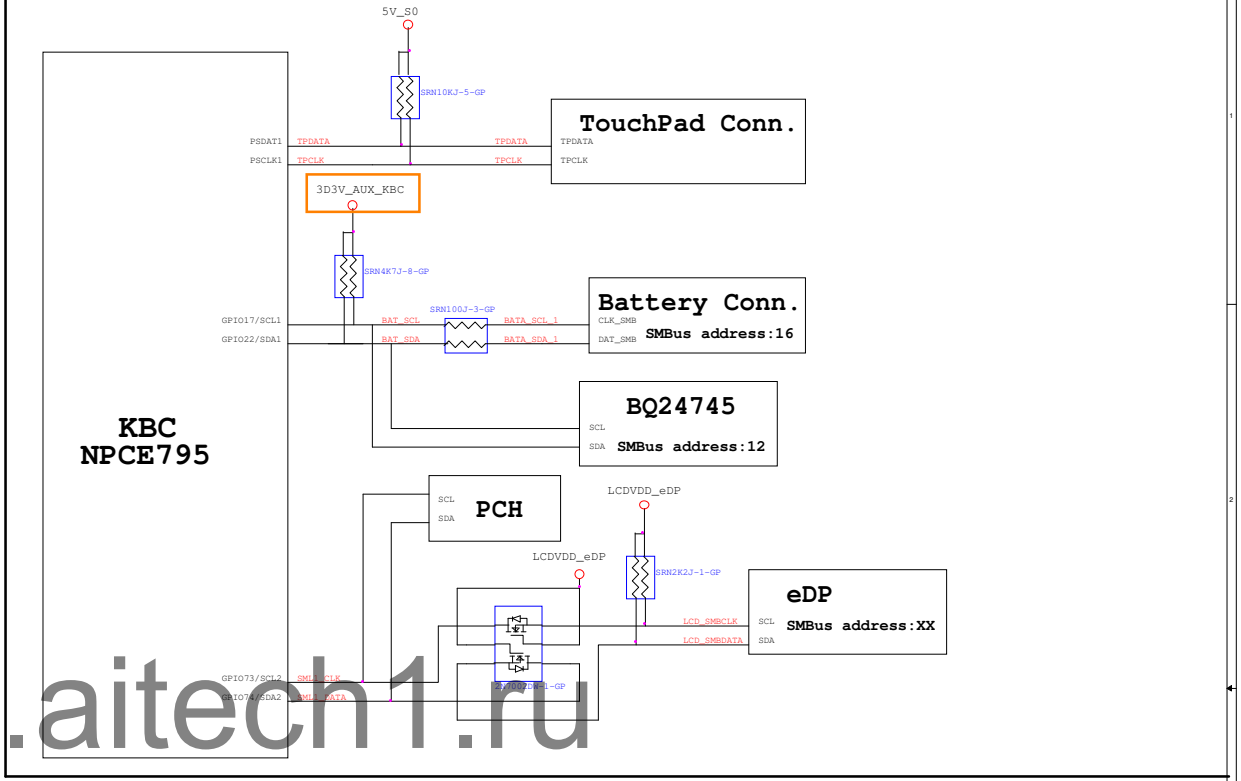
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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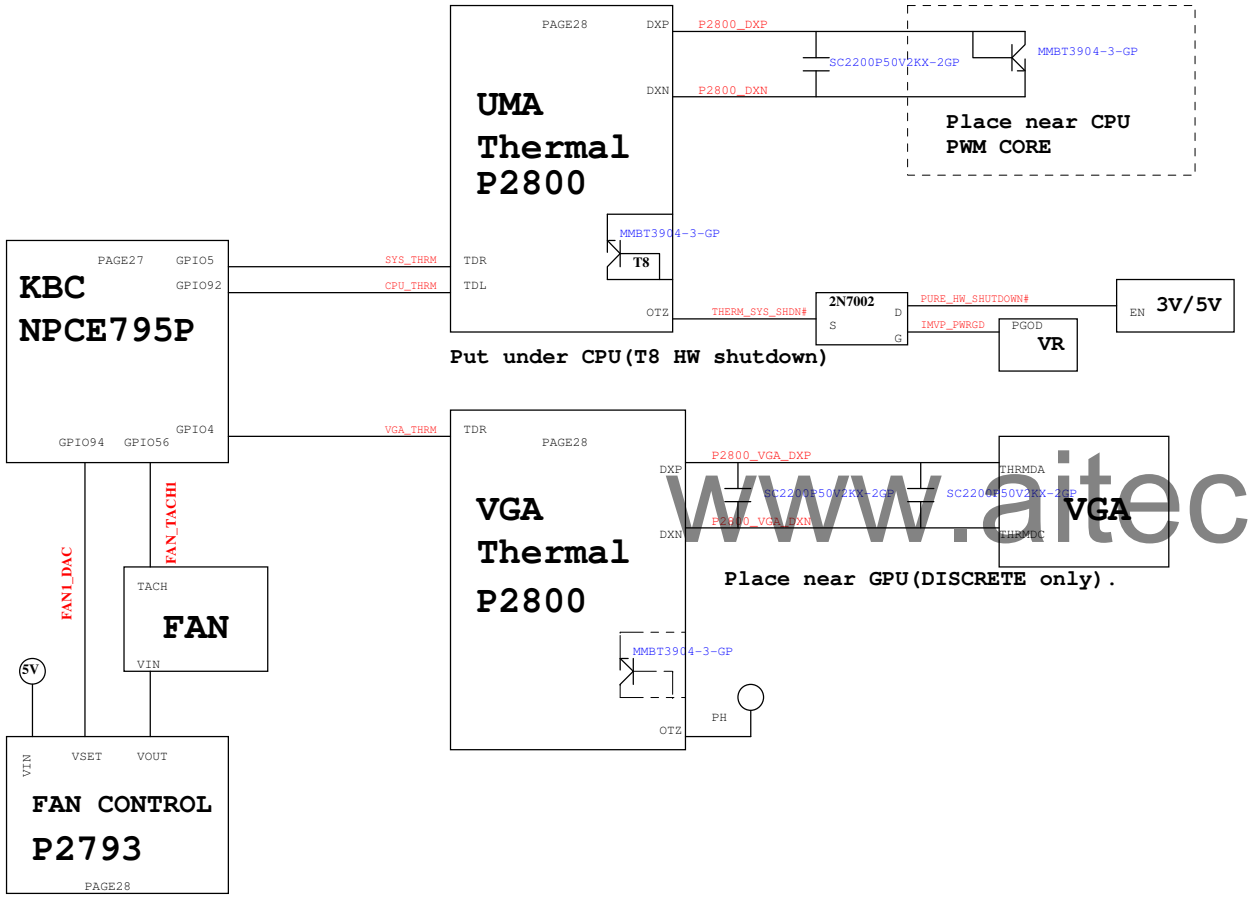
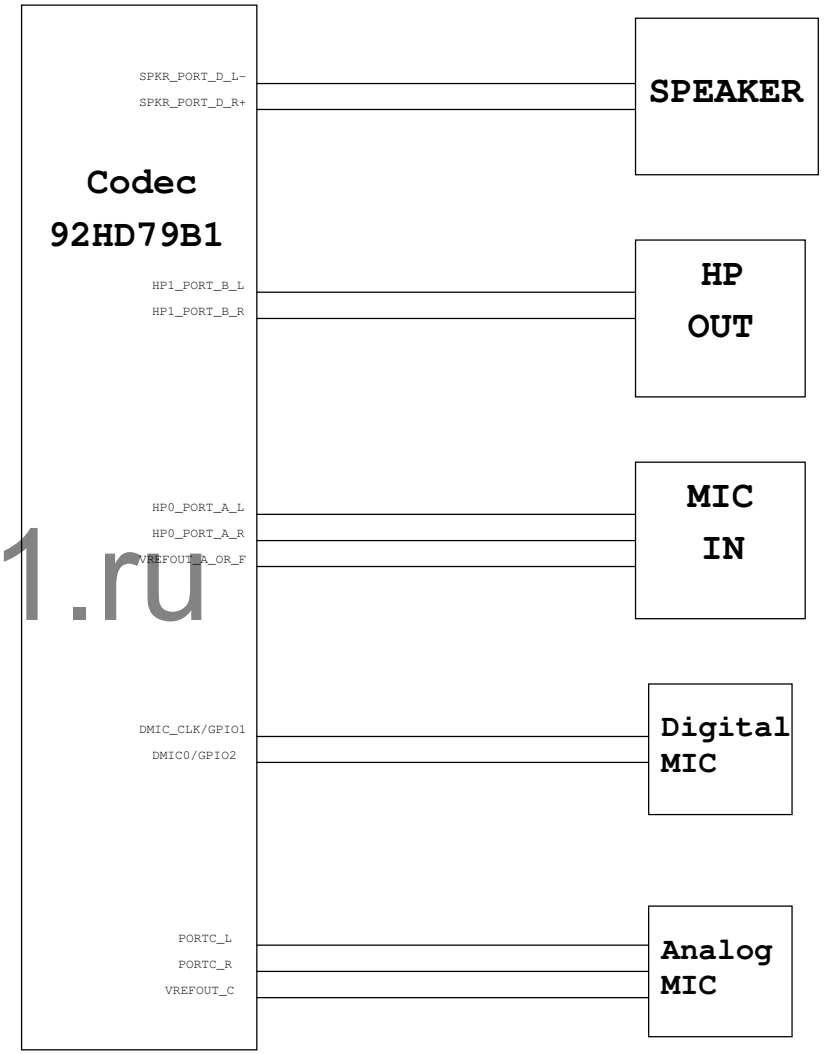
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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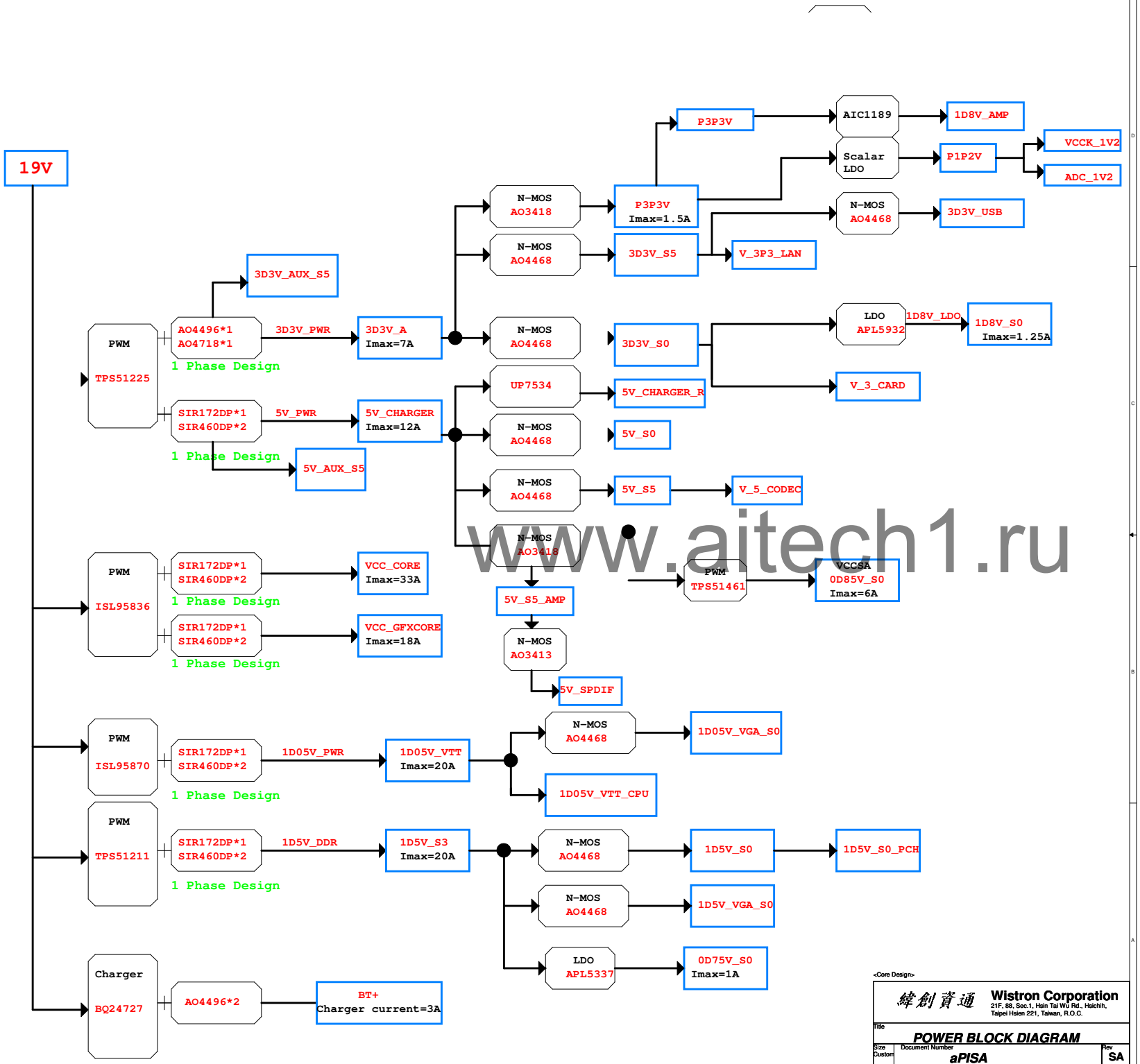

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Title: POWER BLOCK DIAGRAM

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